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L4

L2

0

L4

DB=PGPB; PLUR=YES; OP=OR

L3

L2

0

L3

DB=USPT; PLUR=YES; OP=OR

L2

11 and ((device or module) near5 node)

13

L2

L1

(serial adj1 bus) same (configur\$5 near5 ROM)

19

L1

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side by side		result set	
<i>DB=EPAB; PLUR=YES; OP=OR</i>			
<u>L6</u>	L2	0	<u>L6</u>
<u>L5</u>	L2	0	<u>L5</u>
<i>DB=JPAB; PLUR=YES; OP=OR</i>			
<u>L4</u>	L2	0	<u>L4</u>
<i>DB=PGPB; PLUR=YES; OP=OR</i>			
<u>L3</u>	L2	0	<u>L3</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L2</u>	11 and ((device or module) near5 node)	13	<u>L2</u>
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Set Name Query

side by side

Hit Count Set Name

result set

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DB=PGPB; PLUR=YES; OP=OR			
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DB=USPT; PLUR=YES; OP=OR			
<u>L2</u>	11 and ((device or module) near5 node)	13	<u>L2</u>
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(configuration adj1 ROM) same
(serial adj1 bus)

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2	<input type="checkbox"/>	<input type="checkbox"/>	US 6334161 B1	20011225	85	System for reverse data transmission flow contr	710
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6237049 B1	20010522	30	Method and system for defining and discoverin	710
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bus and configur* and ROM

[Search Again](#)**Results:**Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD****1 A reusable microcontroller core's design***Janiszewki, I.; Baraniecki, R.; Siekierska, K.*

Fall VIUF Workshop, 1999. , 1999

Page(s): 14 -19

[\[Abstract\]](#) [\[PDF Full-Text \(636 KB\)\]](#) **CNF**
2 IEEE standard for boot (initialization configuration)**firmware: bus supplement for IEEE 896 (Futurebus+)**
 IEEE Std 1275.4-1995 (IEEE standard for boot (initialization configuration) firmware: bus supplement for IEEE 896 (Futurebus+))
 , 27 Feb. 1996

[\[Abstract\]](#) [\[PDF Full-Text \(724 KB\)\]](#) **STD**
3 IEEE standard for boot (initialization configuration)**firmware: instruction set architecture (ISA) supplement for IEEE 1754**

IEEE Std 1275.1-1994 , 18 Nov. 1994

[\[Abstract\]](#) [\[PDF Full-Text \(528 KB\)\]](#) **STD**
4 IEEE standard for boot (initialization configuration)**firmware: Bus supplement for IEEE 1496 (SBus)**

IEEE Std 1275.2-1994 , 18 Nov. 1994

[\[Abstract\]](#) [\[PDF Full-Text \(472 KB\)\]](#) **STD**
5 A large scale FPGA with 10 K core cells with CMOS 0.8 mu m 3-layered metal process*Muroga, H.; Murata, H.; Saeki, Y.; Hibi, T.; Ohashi, Y.; Noguchi, T.;*

Nishimura, T.

Custom Integrated Circuits Conference, 1991., Proceedings of the
IEEE 1991 , 1991

Page(s): 6.4/1 -6.4/4

[\[Abstract\]](#) [\[PDF Full-Text \(188 KB\)\]](#) **CNF**

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CITATION

A reusable microcontroller core's design
- Janiszewki, I. Baraniecki, R. Siekierska, K.
Inst. of Electron Technol., Warsaw, Poland
This paper appears in: Fall VIUF Workshop, 1999.

On page(s): 14 - 19

4-6 Oct. 1999

Orlando, FL, USA

1999

ISBN: 0-7695-0465-5

IEEE Catalog Number: PR00465

Number of Pages: ix+110

References Cited: 4

INSPEC Accession Number: 6409772

Abstract:

The paper concerns a configurable soft core of the 8051 /spl mu/C implemented in VHDL. The main goal of efforts undertaken during design of the core was the full compatibility with the industrial standards 80C51 and 80C52 on the instruction and timing levels. It doesn't limit flexibility of the core's architecture, which can be easily optimized according to the current design constraints. The configuration capabilities of the core are grouped in a configuration package. That approach allows for separation from the indigenous part of the core, which remains untouched by a user and can be encoded in order to hide the VHDL code. Inside the configuration package there are several constants. Assigning values to them, a user has the opportunity to determine the core's structure (types of functional modules used in the core), RAM and ROM sizes, the instruction set, number of interrupted sources, number of execution cycles for division and multiplication, etc. The core is independent of the CPU peripheral modules (e.g. timer/counters, I/O ports, UART, etc.) due to a SFR bus. Peripherals are accessed by the use of special function registers. The upper half of available addresses of the internal RAM is just reserved for them. Hence the communication between the CPU and SFRs is carried out in the same way as in the case of memory cells. The core has been proven on silicon. It was applied in the smart pressure sensor chip and an 8031-compatible /spl mu/C. The compatibility with the industrial was checked on the logic verifier, where original 80C51 and 80C52 chips were applied during tests as references.

Index Terms:

microcontrollers hardware description languages configuration management standards instruction sets reusable microcontroller core design configurable soft core 8051 /spl mu/C functional modules industrial standards 80C51 80C52 timing levels design constraints configuration capabilities configuration package VHDL code ROM sizes instruction set interrupted sources execution cycles CPU peripheral

modules SFR bus special function registers internal RAM smart
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 Bus Architecture Standards Committee of the IEEE Computer Society, USA

This paper appears in: IEEE Std 1275.4-1995 (IEEE standard for boot (initialization configuration) firmware: bus supplement for IEEE 896 (Futurebus+))
 IEEE Std 1275.4-1995
 27 Feb. 1996

IEEE Catalog Number:
 Number of Pages: v+10
 References Cited: 5
 INSPEC Accession Number: 5261314

Abstract:

Firmware is the read-only-memory (ROM)-based software that controls a computer between the time it is turned on and the time the primary operating system takes control of the machine. Firmware's responsibilities include testing and initializing the hardware, determining the hardware configuration, loading (or booting) the operating system, and providing interactive debugging facilities in case of faulty hardware or software. The core requirements and practices specified by IEEE Std 1275-1994 must be supplemented by system-specific requirements to form a complete specification for the firmware for a particular system. This standard establishes such additional requirements pertaining to the bus architecture defined by the IEEE Futurebus+ standards: ISO/IEC 10857: 1994 [ANSI/IEEE Std 896.1, 1994 Edition], Information technology-Microprocessor systems-Futurebus+-Logical protocol specification; and IEEE Std 896.2-1991, IEEE Standard for Future+-Physical Layer and Profile Specification.

Index Terms:

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INSPEC Accession Number: 5261314

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Firmware is the read-only-memory (ROM)-based software that controls a computer between the time it is turned on and the time the primary operating system takes control of the machine. Firmware's responsibilities include testing and initializing the hardware, determining the hardware configuration, loading (or booting) the operating system, and providing interactive debugging facilities in case of faulty hardware or software. The core requirements and practices specified by IEEE Std 1275-1994 must be supplemented by system-specific requirements to form a complete specification for the firmware for a particular system. This standard establishes such additional requirements pertaining to the bus architecture defined by the IEEE Futurebus+ standards: ISO/IEC 10857: 1994 [ANSI/IEEE Std 896.1, 1994 Edition], Information technology-Microprocessor systems-Futurebus+-Logical protocol specification; and IEEE Std 896.2-1991, IEEE Standard for Future+-Physical Layer and Profile Specification.

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L2: Entry 1 of 13

File: USPT

Mar 5, 2002

DOCUMENT-IDENTIFIER: US 6353868 B1

TITLE: Digital camera controlling communication by multiple function units

Brief Summary Paragraph Right (12):

It is another object of the present invention to provide an electronic equipment and interface control device capable of communications with various nodes via various interfaces.

Detailed Description Paragraph Right (19):

The first 512 bytes of the register space include a kernel of a known CSR architecture, and the next 512 bytes are used as a serial bus register. The specific contents of these areas are well known and the detailed description thereof is omitted. These areas and the next 1024-byte configuration ROM and a portion of a unit space are implemented on each equipment.

Detailed Description Paragraph Right (65):

It is assumed that the electronic equipment of this embodiment having the structure shown in FIG. 7 operates as the digital moving image camera/recorder and communicates with another node by supplying node information onto the 1394 bus 13 via the 1394 serial bus I/F circuit 5, under the first subsidiary communication protocol stored in the first configuration ROM (CR1) 8.

Detailed Description Paragraph Right (85):

The digital still image camera/recorder (second unit) is reconfigured and the C & S register 10 is set for use with the digital still image camera/recorder. Next, in order to change the node information of the 1394 serial bus I/F circuit 5 from the first configuration ROM 8 to the second configuration ROM 9, the address setting of the I/F control and address conversion circuit 7 is changed. Namely, since the configuration ROMs 8 and 9 are located at different addresses in the above-described address space, the address setting is changed to select the second configuration ROM 9.

Detailed Description Paragraph Right (86):

Thereafter, in order to reconfigure the management configuration of the 1394 serial bus 13 under the reset state, the bus interconnection of the 1394 serial bus I/F circuit 5 is recovered. In this manner, the electronic equipment of this embodiment is newly defined as the digital still image camera/recorder having the still image subsidiary communication protocol, in accordance with the new bus management configuration and the node information in the second configuration ROM 9. This new definition is detected by the root node which controls the bus management of the system shown in FIG. 5, and therefore recognized by the system.

Detailed Description Paragraph Right (92):

If changed to the digital video (moving image camera/recorder), the flow advances to Step S4 to perform the unit control corresponding to the system configuration of the digital video, at Step S5 the C & S register 10 is set for use with the digital video, and at Step S6 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the first configuration ROM 8.

Detailed Description Paragraph Right (93):

If it is judged at Step S3 that the equipment has been changed to the digital camera (still image camera/recorder), the flow advances to Step S7 to perform the unit

control corresponding to the system configuration of the digital camera, at Step S8 the C & S register 10 is set for use with the digital camera, and at Step S9 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the second configuration ROM 9.

Detailed Description Paragraph Right (94):

After the processes at Steps S4 to S6 or Steps S7 to S9, the reset state of the 1394 serial bus 13 started at Step S2 is released to recover the bus connection of the 1394 serial bus I/F circuit 5. At Step S11 the root node executes a new bus management process after the system change and recognizes the equipment of this embodiment either as the moving image camera/recorder having the AV/C protocol or as the still image camera/recorder having the still image subsidiary communication protocol, in accordance with the contents of the configuration ROM 8 or 9.

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L2: Entry 1 of 13

File: USPT

Mar 5, 2002

US-PAT-NO: 6353868

DOCUMENT-IDENTIFIER: US 6353868 B1

TITLE: Digital camera controlling communication by multiple function units

DATE-ISSUED: March 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takayama; Nobutoshi	Yokohama			JPX
Itou; Masamichi	Tokyo			JPX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JPX	03

APPL-NO: 9/ 614547 [PALM]

DATE FILED: July 12, 2000

PARENT-CASE:

This application is a division of application Ser. No. 09/414,319, filed Oct. 7, 1999, now U.S. Pat. No. 6,138,196, which is a division of application Ser. No. 08/917,295, filed Aug. 25, 1997, now U.S. Pat. No. 5,991,842.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-225183	August 27, 1996

INT-CL: [7] G06 F 13/00, G06 F 13/42

US-CL-ISSUED: 710/129; 710/105, 710/106, 710/62, 710/11, 358/1.15

US-CL-CURRENT: 358/1.15, 710/105, 710/106, 710/11, 710/62

FIELD-OF-SEARCH: 710/105, 710/104, 710/106, 710/11, 710/62, 710/101, 710/129, 348/220, 709/238, 370/463, 370/912, 358/1.15

PRIOR-ART-DISCLOSED:

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<input type="checkbox"/>	<u>6195243</u>	February 2001	Spencer et al.	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper & Scinto

ABSTRACT:

An electronic equipment for communications with other nodes via a serial bus interface. The electronic equipment has a plurality of functions, and stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the serial bus interface. An interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

64 Claims, 12 Drawing figures

WEST☐

L2: Entry 2 of 13

File: USPT

Dec 25, 2001

DOCUMENT-IDENTIFIER: US 6334161 B1

TITLE: System for reverse data transmission flow control wherein command is transferred by asynchronous transfer mode while data is transferred by isochronous transfer mode

Drawing Description Paragraph Right (30):

FIG. 26D is an example of a minimum format of a configuration ROM of the 1394 serial bus;

Drawing Description Paragraph Right (31):

FIG. 26E is an example of a general format of the configuration ROM of the 1394 serial bus;

Detailed Description Paragraph Right (13):

FIG. 3 shows address space of the 1394 serial bus. All the devices (nodes) connected to the 1394 serial bus have a unique 64 bit address. The 64 bit address is stored in a memory of the devices. Data communication with a designated destination device can be performed by always recognizing the node addresses of the transmitting- and receiving-side nodes.

Detailed Description Paragraph Right (16):

In the register space, the initial 512 bytes are assigned to a register core (CSR core) as a core of a Command/Status Register (CSR) architecture; the next 512 bytes, to a register of the serial bus; the next 1024 bytes, to a configuration ROM; and the remaining bytes, to a register unique to the device in a unit space.

Detailed Description Paragraph Right (17):

Generally, for the sake of simplification of bus system design for different node types, it is preferable that only the initial 2048 are used for the nodes, and as a result, total 4096 bytes are used including the initial 2048 bytes for the CSR core, the register of the serial bus, the configuration ROM and the unit space.

Detailed Description Paragraph Right (22):

The respective devices (nodes) connected to the 1394 serial bus are provided with a node ID, and are recognized as nodes constructing the network. For example, when increase/decrease of the number of nodes due to connection/disconnection or power ON/OFF status of network devices, i.e., network construction changes and it is necessary to recognize a new network construction, the respective nodes detect the change of network construction, send a bus-reset signal onto the bus, and enter a mode for recognizing the new network construction. The detection of change of network construction is made by detecting change of bias voltage at the connector port 810.

Detailed Description Paragraph Right (188):

FIG. 45 shows a register map of registers necessary for the transfer method 1 and the transfer method 2, in address space of the 1394 serial bus. In the present embodiment, a node on the controller side is the image providing device (controller in the FCP protocol), and a node on the controlled side is the printer (target in the FCP protocol).

WEST☐ **Generate Collection** **Print**

L2: Entry 2 of 13

File: USPT

Dec 25, 2001

US-PAT-NO: 6334161

DOCUMENT-IDENTIFIER: US 6334161 B1

TITLE: System for reverse data transmission flow control wherein command is transferred by asynchronous transfer mode while data is transferred by isochronous transfer mode

DATE-ISSUED: December 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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Tateyama; Jiro	Yokohama			JPX
Nakamura; Atsushi	Kawasaki			JPX
Kobayashi; Makoto	Yokohama			JPX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JPX	03

APPL-NO: 9/ 024160 [PALM]

DATE FILED: February 17, 1998

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	9-030982	February 14, 1997
JP	9-166433	June 23, 1997
JP	9-166434	June 23, 1997

INT-CL: [7] G06 F 15/16, G06 F 13/00, G06 F 13/14, G06 F 13/42, G06 F 9/06

US-CL-ISSUED: 710/29; 710/5, 710/15, 710/31, 710/32, 710/33, 710/12, 710/105, 710/107, 710/110, 710/11, 710/8, 709/212, 709/213, 709/231, 714/36, 714/746

US-CL-CURRENT: 710/29; 709/212, 709/213, 709/231, 710/105, 710/107, 710/11, 710/110, 710/12, 710/15, 710/31, 710/32, 710/33, 710/5, 710/8, 714/36, 714/746

FIELD-OF-SEARCH: 710/51, 710/29, 710/12, 710/52, 710/117, 710/105, 710/15, 710/8, 710/5, 710/31, 710/32, 710/33, 710/110, 710/107, 710/11, 709/212, 709/213, 709/231, 714/746, 714/36, 358/406, 370/461

PRIOR-ART-DISCLOSED:

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Search Selected**Search ALL**

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WO 87/01484	March 1987	WOX	
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Teener, "A Bus on a Diet--The Serial Bus Alternative" Intellectual Leverage, Feb. 24, 1992, No. Conf. 37, pp. 316-321.

ART-UNIT: 272

PRIMARY-EXAMINER: Lee; Thomas

ASSISTANT-EXAMINER: Schuster; Katharina

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper, & Scinto

ABSTRACT:

A host computer logs in an image providing device such as a scanner connected by a serial bus, and reverses flow control of data transfer by issuing a Reverse command. The image providing device opens a transfer channel by an OpenChannel command, transfers image data in form of blocks. When the transfer of the image data has been completed, the image providing device closes the transfer channel by a CloseChannel command, and reverses the flow control of the data transfer again by the Reverse command. This changes the data transfer direction of a device having a bi-directional data transfer function, i.e., a device having a data reception function and a data providing function.

46 Claims, 77 Drawing figures



☐ Generate Collection Print

L2: Entry 3 of 13

File: USPT

May 22, 2001

DOCUMENT-IDENTIFIER: US 6237049 B1

TITLE: Method and system for defining and discovering proxy functionality on a distributed audio video network

Brief Summary Paragraph Right (3):

Recently, a class of consumer electronic media devices has been introduced that can be networked together using a standard communication protocol layer (e.g., IEEE 1394 communication standard). The IEEE 1394 standard is an international standard for implementing an inexpensive high-speed serial bus architecture which supports both asynchronous and isochronous format data transfers. The IEEE 1394 standard provides a high-speed serial bus for interconnecting digital devices thereby providing universal input/output connection. The IEEE 1394 standard defines a digital interface for applications thereby eliminating the need for an application to covert digital data to an analog form before it is transmitted across the bus. Correspondingly, a receiving application will receive digital data from the bus, not analog data and will therefore not be required to convert analog data to digital form. The IEEE 1394 standard is ideal for consumer electronics communication in part because devices can be added to or removed from the serial bus while the bus is active. If a device is so added or removed, the bus automatically reconfigures itself for transmitting data between the then existing devices. Each device on the bus is a "node" and contains its own address space.

Drawing Description Paragraph Right (2):

FIG. 1 illustrates an exemplary networked system of consumer electronic media devices ("nodes") including a video camera, a video cassette recorder, a computer system, a set-top-box, a television, and a compact disc player.

Detailed Description Paragraph Right (5):

FIG. 1 illustrates an exemplary network system 5 that can support the embodiments of the proxy functionality in accordance with the present invention. Exemplary system 5 includes consumer electronic media devices (including computer systems) as nodes but could be extended equally well to cover other electronic devices. System 5 includes a video camera 10, a video cassette recorder (VCR) 12, a computer system 14, a set-top-box 13, a television set (TV) 11, and a compact disc (CD) player 20 connected together with the network by IEEE 1394-1995 (IEEE 1394) cables 15, 16, 17, 18, and 19. The set-top-box 13 can be coupled to receive media from a cable TV system. The IEEE 1394 cable 16 couples the video camera 10 to the VCR 12 allowing the video camera 10 to send data, commands and parameters to the VCR 12 for recording (or to any other-device of network 5). The IEEE 1394 cable 18 couples the VCR 12 to the computer system 14 allowing the VCR 12 to send data, commands and parameters to the computer system 14 for display (or to any other device of network 5).

Detailed Description Paragraph Right (17):

FIG. 3A is a block diagram of memory space referred to as a configuration ROM 302, which is located within each node (e.g., TV 11, VCR 12, set-top-box 13, etc.) of network 5 of FIG. 1. It should be appreciated that configuration ROM 302 of the present invention is defined by the IEEE 1212 specification, which is well known by those of ordinary skill in the art and is the foundation technology of the IEEE 1394 serial bus specification. One embodiment of configuration ROM 302 is a 64 bit memory space that is divided into two different subsections. One subsection contains the upper 16 bits of address space that are used for storing the identification (ID) of a node, which includes its physical identification (phyID) 304. The other subsection within configuration ROM 302 contains the remaining 48 bits of address space that are

used for storing other configuration ROM data structures 306 pertaining to the specific node, e.g., its Global Unique Identification (GUID) value. In this manner, an IEEE 1394 serial bus network of the present invention is a memory mapped bus network. It should be appreciated that a proxy data structure 330 is typically stored within the 48 bits of address space along with the other data structures 306 of configuration ROM 302, in accordance with the present invention. The proxy data structure 330 is described in more detail below with reference to FIGS. 3C and 3D. It should be further appreciated that there are many other embodiments of the configuration ROM 302 in accordance with the present invention. For example, the configuration ROM 302 can be implemented using RAM, static RAM, dynamic RAM, programmable ROM, flash memory, EPROM, EEPROM, or any other memory device.

Detailed Description Paragraph Right (20):

The proxy tag 332 of FIG. 3C, in accordance with the present invention, is a recognizable tag to other nodes of network 5 indicating that proxy device 13 is a proxy for a particular node (e.g., VCR 12). It should be appreciated that proxy tag 332 should be defined within the IEEE 1212r specification, in accordance with the present invention. In this manner, all other consumer electronic devices that are coupled together by an IEEE 1394 serial bus will, by definition, recognize proxy tag 332 when they search the configuration ROM of proxy device 13, regardless of whatever higher level protocols (e.g., AV/C, HAVi, etc.) they support. The length 334 indicates the amount of bytes that correspond to the proxy identifier 336.

Detailed Description Paragraph Right (21):

The proxy identifier 336 of FIG. 3C contains data indicating the specific identity of the node within network 5 for which proxy device 13 is acting as a proxy. One method of identifying the specific node in accordance within the present invention is to utilize the phyID of the node along with other IEEE 1212r data structure information. Another method of identifying the specific node in accordance within the present invention is to utilize the GUID of the node along with the node's functionality information. It should be appreciated that other information can be stored within proxy identifier 336. For instance, the proxy identifier 336 can also include data indicating a particular proxy service or services (e.g., data library, translator, arbitrator, etc.) that proxy device 13 provides for another node (e.g., VCR 12). Furthermore, the proxy identifier 336 can also include data indicating that proxy device 13 is a proxy for a particular (e.g., AV/C) subunit or subunits of another node. Moreover, the proxy identifier 336 can also include data indicating that proxy device 13 is a proxy for a particular (e.g., IEEE 1212) unit directory of another node.

Detailed Description Paragraph Right (22):

Therefore, by reading the configuration ROM 302 of proxy device 13, the other nodes (devices) of network 5 within the present embodiment are able to determine that proxy device 13 is acting as a proxy for another node (e.g., VCR 12), the proxy services that the proxy device 13 provides on behalf of that node, and the particular protocol of those proxy services.

Detailed Description Paragraph Right (25):

In the present invention, there is another method for enabling a proxy device (e.g., set-top-box 13 of FIG. 2A) to identify itself as a proxy to all other consumer electronic media devices of network 5. Specifically, proxy device 13 can represent itself as a proxy for another node of network 5 within an IEEE 1212 Unit Directory structure, which is stored within one of its memory units. It should be appreciated that the IEEE 1212 Unit Directory structure is well known by those of ordinary skill in the art. Within one embodiment of the IEEE 1212 Unit Directory structure, in accordance with the present invention, is stored information indicating the identity of the node within network 5 for which proxy device 13 is acting as a proxy, the proxy services or capabilities it provides on behalf of that node, and the protocol of the particular proxy services. It should be further appreciated that the identity of the node can be specified using any of the methods described above or by using the GUID of the node along with a unique identifier of the unit directory within that node. The identifying reference of the node is stored within the unit directory of proxy device 13.

Detailed Description Paragraph Right (30):

FIG. 5 is a flowchart illustrating steps of a process 500 for establishing a proxy consumer electronic media device as a proxy for other consumer electronic media devices in accordance with one embodiment of the present invention. It should be appreciated that process 500 is one embodiment of step 404 of FIGS. 4A and 4B, in accordance with the present invention. Process 500 is realized as program code stored within computer readable memory units of a proxy consumer electronic media device and other consumer electronic media devices of network 5. Process 500 begins at step 502 and at step 504, the proxy device discovers a consumer electronic media device which is coupled to the IEEE 1394 serial bus. This process utilizes well known IEEE 1394 communication protocol mechanisms. At step 506, the proxy device determines the functional capabilities of the located consumer electronic media device. One method in accordance with the present invention for the proxy device to perform step 506 is to read all of the configuration ROM within the located consumer electronic media device, which is a well known IEEE 1212 communication protocol mechanism.

WEST☐

L2: Entry 3 of 13

File: USPT

May 22, 2001

US-PAT-NO: 6237049

DOCUMENT-IDENTIFIER: US 6237049 B1

TITLE: Method and system for defining and discovering proxy functionality on a distributed audio video network

DATE-ISSUED: May 22, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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ASSIGNEE-INFORMATION:

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Sony Electronics, Inc.	Park Ridge	NJ			02

APPL-NO: 9/ 151373 [PALM]

DATE FILED: September 10, 1998

PARENT-CASE:

CROSS REFERENCE TO RELATED APPLICATIONS This is a continuation-in-part of U.S. application Ser. No. 09/003,119, now U.S. Pat. No. 6,032,202 entitled "Home Audio/Video Network with Two Level Device Control" by Rodger J. Lea et al., filed Jan. 6, 1998.

INT-CL: [7] H04 N 7/173

US-CL-ISSUED: 710/8; 725/118, 725/120, 725/131, 725/134

US-CL-CURRENT: 710/8; 725/118, 725/120, 725/131, 725/134

FIELD-OF-SEARCH: 348/8, 348/6, 455/6.2, 455/6.3, 700/8, 700/9, 709/208, 709/217, 709/218, 709/219, 709/213, 709/216, 709/229, 709/249, 340/825.25, 340/825.24, 710/8, 710/101

PRIOR-ART-DISCLOSED:

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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Wray S. et al. "Networked Multimedia: The Medusa Environment"IEEE Multimedia, US, IEEE Computer Society, vol. 1, No. 4, pp. 54-63.

ART-UNIT: 261
PRIMARY-EXAMINER: Faile; Andrew
ASSISTANT-EXAMINER: Bui; Kieu-Oanh
ATTY-AGENT-FIRM: Wagner, Murabito & Hao LLP

ABSTRACT:

A method and system for defining and discovering proxy functionality on a distributed audio video network. The present invention operates within a network of consumer electronic media devices (e.g., television, set-top-box, video cassette recorder, compact disc device, personal computer system, etc.) that are coupled together using the IEEE 1394 serial communication standard. Specifically, the present invention enables a consumer electronic media device having increased functionality to act as a proxy device for other consumer electronic media devices. As such, the proxy device is able to provide a wide variety of advantageous proxy services for other consumer electronic media devices thereby increasing their original capabilities. For instance, the proxy device can act as a translator between two devices thereby enabling them to communicate. Additionally, the proxy device can enable Home Audio Video Interoperability (HAVi) devices to have greater control over non-HAVi devices. Moreover, the proxy device can extend the existing functionality of devices as well as provide new functionality for them. Furthermore, the proxy device can act as a command arbitrator for particular devices. Also, the proxy device can act as a proxy for all or a portion of the functionality of a device. It is appreciated that these are only examples of the possible advantageous proxy services that the proxy device can provide for other devices in accordance with the present invention.

37 Claims, 18 Drawing figures

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L2: Entry 6 of 13

File: USPT

Oct 24, 2000

DOCUMENT-IDENTIFIER: US 6138196 A

TITLE: Communication system for providing digital data transfer, electronic equipment for transferring data using the communication system, and an interface control device

Brief Summary Paragraph Right (12):

It is another object of the present invention to provide an electronic equipment and interface control device capable of communications with various nodes via various interfaces.

Detailed Description Paragraph Right (19):

The first 512 bytes of the register space include a kernel of a known CSR architecture, and the next 512 bytes are used as a serial bus register. The specific contents of these areas are well known and the detailed description thereof is omitted. These areas and the next 1024-byte configuration ROM and a portion of a unit space are implemented on each equipment.

Detailed Description Paragraph Right (65):

It is assumed that the electronic equipment of this embodiment having the structure shown in FIG. 7 operates as the digital moving image camera/recorder and communicates with another node by supplying node information onto the 1394 bus 13 via the 1394 serial bus I/F circuit 5, under the first subsidiary communication protocol stored in the first configuration ROM (CR1) 8.

Detailed Description Paragraph Right (80):

The digital still image camera/recorder (second unit) is reconfigured and the C & S register 10 is set for use with the digital still image camera/recorder. Next, in order to change the node information of the 1394 serial bus I/F circuit 5 from the first configuration ROM 8 to the second configuration ROM 9, the address setting of the I/F control and address conversion circuit 7 is changed. Namely, since the configuration ROMs 8 and 9 are located at different addresses in the above-described address space, the address setting is changed to select the second configuration ROM 9.

Detailed Description Paragraph Right (81):

Thereafter, in order to reconfigure the management configuration of the 1394 serial bus 13 under the reset state, the bus interconnection of the 1394 serial bus I/F circuit 5 is recovered. In this manner, the electronic equipment of this embodiment is newly defined as the digital still image camera/recorder having the still image subsidiary communication protocol, in accordance with the new bus management configuration and the node information in the second configuration ROM 9. This new definition is detected by the root node which controls the bus management of the system shown in FIG. 5, and therefore recognized by the system.

Detailed Description Paragraph Right (87):

If changed to the digital video (moving image camera/recorder), the flow advances to Step S4 to perform the unit control corresponding to the system configuration of the digital video, at Step S5 the C & S register 10 is set for use with the digital video, and at Step S6 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the first configuration ROM 8.

Detailed Description Paragraph Right (88):

If it is judged at Step S3 that the equipment has been changed to the digital camera

(still image camera/recorder), the flow advances to Step S7 to perform the unit control corresponding to the system configuration of the digital camera, at Step S8 the C & S register 10 is set for use with the digital camera, and at Step S9 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the second configuration ROM 9.

Detailed Description Paragraph Right (89):

After the processes at Steps S4 to S6 or Steps S7 to S9, the reset state of the 1394 serial bus 13 started at Step S2 is released to recover the bus connection of the 1394 serial bus I/F circuit 5. At Step S11 the root node executes a new bus management process after the system change and recognizes the equipment of this embodiment either as the moving image camera/recorder having the AV/C protocol or as the still image camera/recorder having the still image subsidiary communication protocol, in accordance with the contents of the configuration ROM 8 or 9.

WEST☐ **Generate Collection** **Print**

L2: Entry 6 of 13

File: USPT

Oct 24, 2000

US-PAT-NO: 6138196

DOCUMENT-IDENTIFIER: US 6138196 A

TITLE: Communication system for providing digital data transfer, electronic equipment for transferring data using the communication system, and an interface control device

DATE-ISSUED: October 24, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takayama; Nobutoshi	Yokohama			JPX
Itou; Masamichi	Tokyo			JPX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JPX	03

APPL-NO: 9/ 414319 [PALM]

DATE FILED: October 7, 1999

PARENT-CASE:

This application is a division of application Ser. No. 08/917,295 filed Aug. 25, 1997, now U.S. Pat. No. 5,991,842.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-225183	August 27, 1996

INT-CL: [7] G06 F 13/00, G06 F 13/42

US-CL-ISSUED: 710/105; 710/104, 710/106, 710/11, 710/62

US-CL-CURRENT: 710/105; 710/104, 710/106, 710/11, 710/62

FIELD-OF-SEARCH: 710/105, 710/104, 710/106, 710/11, 710/62, 710/101, 710/129, 709/238, 709/253, 370/463, 370/912, 379/88.13

PRIOR-ART-DISCLOSED:

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<input type="checkbox"/>	<u>6038625</u>	March 2000	Ogino et al.	

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper & Scinto

ABSTRACT:

An electronic equipment for communications with other nodes via a serial bus interface. The electronic equipment has a plurality of functions, and stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the serial bus interface. An interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

11 Claims, 12 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 10

BRIEF SUMMARY:

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an interface control device, an electronic equipment, and a communication system, and more particularly to a communication system for digital data transfer using a serial bus interface, an electronic equipment for digital data transfer using such a system, and a control device for controlling such a system.

2. Related Background Art

With the development of recent multimedia techniques, various types of data in various formats can be transferred via one digital I/F (interface) system under various communication protocols.

There is an equipment capable of using only one communication protocol although it has a plurality of functional units, in which each unit can be externally controlled and can transfer data to and from external devices. One of digital I/F bus systems of this kind is an IEEE 1394 serial bus.

In order to deal with nodes having various functions, the IEEE 1394 serial bus is generally provided with, in addition to a protocol common to IEEE 1394, other

different communication protocols. In this specification, a common protocol independent from functional units of each equipment, although it is specific to each serial bus such as IEEE 1394 serial bus, is called a fundamental protocol, whereas a protocol dependent upon each functional unit is called a subsidiary communication protocol.

Specifically, even for digital data communications in conformity with the fundamental protocol of a digital I/F bus system, it is generally necessary that a subsidiary communication protocol defined for each node terminal (I/F terminal) matches the protocol of the communication partner, and the communication partner is required to have means for converting the format of received data into a format usable at the communication partner.

The subsidiary communication protocol is generally standardized in accordance with the genre (category) of each equipment or its unit. Therefore, each node has been generally configured as an equipment compatible with a single subsidiary communication protocol.

Definition (definition of node information) of an equipment as viewed from a digital I/F bus has been difficult to generate if a plurality of functions provided by the equipment cannot be operated at the same time, or if the unit configuration or the subsidiary communication protocol changes because of connecting a new unit or attachment.

Even if an equipment is an image input equipment having only a single function, the input image may be used in a different manner at the communication partner. In such a case, it is desired that subsidiary communication protocols different for each use type such as displaying, recording and printing are separately prepared. It is also necessary to consider that a different subsidiary communication protocol may be used by each manufacture of the equipment, even if both the function and use type are the same.

SUMMARY OF THE INVENTION

The invention has been made under the above circumstances, and aims at configuring a communication system while considering a node having various functions and various use types of a digital interface.

It is another object of the present invention to provide an electronic equipment and interface control device capable of communications with various nodes via various interfaces.

In order to achieve the above objects of the invention, an electronic equipment of one embodiment has a plurality of functions and stores a plurality piece of information representative of a plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the digital serial bus interface.

According to another embodiment of the invention, an interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

An electronic equipment or interface control device according to another embodiment of the invention, selectively reads information from another equipment which stores information on a plurality of functions or information on a plurality of subsidiary communication protocols. Therefore, the communication system can perform communications most suitable for each function.

A communication system of the invention stores a plurality of information representative of a plurality of functions provided by each electronic equipment, and selectively reads the information so that the function corresponding to the read

information can be realized at the electronic equipment and optimum communications can be performed.

The other objects and features of the invention will become apparent from the following detailed description of embodiments when read in conjunction with the accompanying drawings.

DRAWING DESCRIPTION:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram showing an example of a communication system configured by using a serial bus of IEEE 1394.

FIG. 2 is a diagram showing the layer structure of a serial bus of IEEE 1394.

FIG. 3 is a diagram illustrating an address space allocation of a serial bus of IEEE 1394.

FIG. 4 is a diagram showing the contents of a configuration ROM, addresses being allocated in the manner illustrated in FIG. 3.

FIG. 5 is a diagram showing the configuration of a communication system according to an embodiment of the invention.

FIG. 6 is a diagram illustrating communication cycles of the system shown in FIG. 5.

FIG. 7 is a diagram showing the detailed structures of a camera/recorder in the system shown in FIG. 5.

FIG. 8 is a diagram illustrating node information stored in a configuration ROM provided in the equipment shown in FIG. 7.

FIG. 9 is a diagram showing a data arrangement in a packet to be transmitted under each subsidiary communication protocol of the equipment shown in FIG. 7.

FIGS. 10A and 10B are diagrams showing the details of the data arrangement shown in FIG. 9.

FIG. 11 is a flow chart illustrating the operation of selecting a function and a subsidiary communication protocol to be executed by the system shown in FIG. 5.

DETAILED DESCRIPTION:

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will be described by using only its preferred embodiments and with reference to the accompanying drawings.

First, a system on which the embodiments are based will be described, this system being a communication system between a plurality of electronic equipments interconnected by serial busses of IEEE-1394-1995 (hereinafter simply called 1394 serial busses).

Communication systems using 1394 serial busses have been proposed as communication systems for multiplex transfer of digital data and control data via digital busses to and from various types of digital equipments such as digital video tape recorders (hereinafter called VTRs) and digital television receivers (hereinafter called TVs).

The 1394 serial bus will be briefly described.

FIG. 1 shows an example of a network system configured by using 1394 serial busses. This system has equipments A, B, C, D, E, F, G and H and twist pair cables of 1394 serial busses interconnecting A and B, A and C, B and B, D and E, C and F, C and G, and C and H. These equipments A to H may be PCs, digital VTRs, DVDs, digital cameras,

hard disks, printers, monitors, and the like.

Interconnection between these equipments can use both a daisy chain scheme and a node branch scheme at the same time, and provides a high degree of connection freedom.

Each equipment has a unique ID so that all the equipments interconnected by 1394 serial busses in one network can be identified. The digital equipments are sequentially connected by a single 1394 serial bus cable, and each equipment provides a repeater function to form one network. A Plug & Play function, which is characteristic of the 1394 serial bus, allows automatic recognition of an equipment and its connection state when it is connected by a cable to the network.

Also in the system shown in FIG. 1, when an equipment is disconnected from the network or a new equipment is added thereto, automatic bus resetting is performed to reset the network configuration and reconfigure a new network. With this function, it is possible to always set and recognize the network configuration at any given time.

The data transfer rates of 100/200/400 Mbps are available, and an equipment having a higher transfer rate supports a lower transfer rate for data transfer compatibility.

The data transfer mode includes an asynchronous transfer mode and an isochronous transfer mode. In the asynchronous transfer mode, asynchronous data (hereinafter described as Async data) such as control signals is transferred, whereas in the isochronous transfer mode, isochronous data (hereinafter described as Iso data) such as real time video data and audio data is transferred. These Async data and Iso data are transferred in a mixed state in each cycle (generally one cycle is 125 .mu.s) after a cycle start packet (CSP) indicating a cycle start is transmitted, while giving the Iso data a priority over the Async data.

FIG. 2 is a schematic diagram showing the functional structure of the 1394 serial bus.

As shown in FIG. 2, the 1394 serial bus is configured as a layer (hierarchical) structure. The constituent at the lowest physical level is a 1394 serial bus cable whose connector is connected to a connector port. At the level higher than this connector port, a physical layer and a link layer are provided as hardware.

This hardware portion is substantially an interface chip. The physical layer of the hardware portion is used for coding, connector control and the like, and the link layer is used for packet transfer, cycle time control and the like.

A transaction layer as firmware is used for the management of transfer data (transaction), and issues commands such as data read and write. A serial bus management manages the connection state and ID of each connected equipment for the node control and network configuration management.

The functions of a bus manager and an isosynchronous resource manager are included in this serial bus management. These hardware and firmware are the fundamental constituents of the 1394 serial bus. Namely, the fundamental protocol of the 1394 serial bus described previously is configured by the firmware up to this transaction layer.

On the other hand, an application layer in a software portion is made of software defined by the above-described subsidiary communication protocols, and changes with each software. Namely, this application layer defines what type of data is transmitted over the 1394 serial bus.

Next, with reference to FIG. 3, addressing of the 1394 serial bus will be described. As shown, an address space of a 64-bit width in conformity with IEEE 1212 regulations is defined for the 1394 serial bus. The first 10 bits of the 64-bit address are called a bus ID which is used for the discrimination between busses. The next 6 bits are called a node ID which is used for the discrimination between equipments. The remaining 48 bits are used as an address space which can be used solely by each equipment.

The 48-bit address space is further divided into a 20-bit field and a 28-bit field. An

area represented by "FFFFF" of the first 20 bits is a register space which is used for information exchange between equipments.

The first 512 bytes of the register space include a kernel of a known CSR architecture, and the next 512 bytes are used as a serial bus register. The specific contents of these areas are well known and the detailed description thereof is omitted. These areas and the next 1024-byte configuration ROM and a portion of a unit space are implemented on each equipment.

The configuration ROM is structured, for example, as shown in FIG. 4 in order to describe the functions of each node. An offset address shown in FIG. 4 indicates a relative address from "FFFFF0000000", and the configuration ROM is located from "FFFFF0000400".

A bus information block (indicated in FIG. 4 by Bus.sub.-- info.sub.-- block) stores data such as an ID of an equipment supply company. A root directory (indicated in FIG. 4 by Root.sub.-- directory) stores information specific to each node and a storage location of the next unit directory (indicated in FIG. 4 by Unit Directory). The unit directory hierarchically stores data representative of the functions of each equipment, data representative of usable subsidiary communication protocols, and other data.

An example of a communication system according to the present invention will be described.

FIG. 5 shows an example of a communication system according to the present invention.

The system shown in FIG. 5 is provided with digital equipments including: a PC (personal computers), a TV, a VTR, and a camera/recorder (hereinafter called a CAM) having a function of picking up a moving image and a still image. 1394 serial buses connect CAM and TV, TV and PC, and PC and VTR. Each of these digital equipments has a function of repeating digital data and control data on the 1394 serial bus.

A cable of a 1394 serial bus is constituted of three sets of shielded paired wires. Paired wires of each set-are used for transfer of protocol signals and data and for supply of electric power. Even if the system has an equipment whose power source is turned off, the operation of the whole system is ensured.

The fundamental structure of each digital equipment, for example, VTR is constituted of: a deck unit; a tuner unit; an operation unit used as user interface; a display unit; a microcomputer for the control of the whole operation, for the generation of communication packets, for the storage of addresses, and the like; a digital interface (digital I/F) unit of 1394 serial buses; and a switch unit for switching between the deck unit, tuner unit, and digital I/F unit. The fundamental structure of TV is constituted of a monitor unit and an amplifier unit in place of the display unit and deck unit of VTR. The fundamental structure of CAM is constituted of a camera unit in place of the tuner unit. The fundamental structure of PC is constituted of a CPU, an operation unit, and an image processing unit, and similar to other digital equipments, of a switch unit and a digital I/F unit.

Communications are performed by using 1394 serial buses at a predetermined communication cycle (125 .mu.s) as illustrated in FIG. 6. Time sequential data such as video data and audio data is transmitted through isochronous communication which ensures a transmission bandwidth at a predetermined data rate, and control data such as control commands is transmitted through asynchronous communication when it becomes necessary.

In such communications, at the start of each communication, a cycle start packet is transmitted, and thereafter packets are transmitted for a predetermined period for isochronous communication.

Packets for isochronous communication are assigned specific channel numbers so that isochronous communication for a plurality of channels can be performed at the same time. For example, assuming that communication from CAM to VTR is assigned a channel number "1", CAM transmits isochronous communication packets of the channel number "1"

immediately after the cycle start packet is transmitted. VTR monitors packets on the bus and picks up packets having the channel number "1" so that isochronous communication between CAM and VTR can be realized.

Similarly, assuming that communication from TV to PC is assigned a channel number "2", each packet of the channel number "2" is transmitted over the bus after each packet of the channel number "1" so that isochronous communication for the channels "1" and "2" can be executed in parallel.

After all isochronous communication packets are transmitted in each communication cycle, the following period until the next cycle start packet is received, is used for asynchronous communication.

Next, bus management allowing the bus system operation will be described.

An equipment operating as a bus manager first retrieves the information on the network configuration and the connection state of all nodes, and gives the definition of each node ID and controls isochronous communication.

In the communication system described above, when a power is turned on, a new digital equipment is connected, or any equipment is disconnected, topology is automatically set by assigning each equipment (node) a node ID (physical address such as #0, #1, #2 and #3 shown in FIG. 5) in accordance with the new interconnection state, as in the following procedure which uses an addressing program and an address table stored in the memory of the microcomputer.

The node ID assigning procedure will be briefly described. This procedure is composed of determination of a system hierarchical structure and assignment of a physical address of each node.

In this example, for the digital equipments described above, it is assumed that TV is a node A, CAM is a node B, PC is a node C, and VTR is a node D.

Each node notifies a partner node connected by the 1394 serial bus that the partner is a parent. In this case, the first notice has a priority. The parent/child relationship of this system is finally determined, namely, the hierarchical structure of the system and a root node which is not a child of any node are determined.

Specifically, in the example shown in FIG. 5, the node D notifies the node C that the node C is a parent, and the node B notifies the node A that the node B is a parent. If the node A notifies the node C that the node C is a parent and the node C notifies the node A that the node A is a parent, the first notice has a priority and if the notice by the node C is faster, the node A is a parent of the node C. In this case, the node A is not a child of any other node and becomes a root node.

After the parent/child relationship of the digital equipments is determined in the above manner, physical addresses are assigned. The basics of physical address assignment are that a parent node gives a child node an address assignment permission and that each child node starting from the node connected to a younger port number is given an address assignment permission.

In the parent/child relationship determined as in the case of FIG. 5, the node A first gives the node B an address assignment permission. Therefore, the node B gives itself a physical address #0. This is notified to the bus to broadcast the effect "physical address #0 already assigned" to all other nodes.

Next, the node A gives the node C an address assignment permission, and then the node D which is a child of the node C is given an address assignment permission. Therefore, the node D gives itself a physical address #1 next to the physical address #0, and notifies this effect to the bus.

Thereafter, the node C assigns itself a physical address #2 and notifies this effect to the bus. Lastly, the node A assigns itself a physical address #3 and notifies this effect to the bus.

Next, the data transfer procedure will be described.

Data transfer becomes possible after the physical addresses are assigned. In the case of 1394 serial buses, however, prior to the data transfer, the root node arbitrates bus use privileges.

If a node wishes to start data transfer, it requests a bus use privilege to the parent node. The root node arbitrates requests for bus use privileges from respective nodes. Prior to data transfer, a node gained the bus use privilege designates a transfer rate and notifies one of 100, 200 and 400 Mbps to a transmission destination node.

Thereafter, in the case of isochronous communication, the transmission originating node starts data transfer at the designated channel immediately after it receives the cycle start packet transmitted synchronously with the communication cycle from the root node operating as a cycle master. The cycle master adjusts the time at each node as well as the transmission of the cycle start packet to the bus.

In the case of asynchronous communication for the transfer of control data such as commands, after the end of isochronous communication in each communication cycle, arbitration for asynchronous communication is performed and then data transfer starts from the transmission originating node to the transmission destination node.

FIG. 7 is a system block diagram showing the detailed structure of the camera/recorder (CAM) shown in FIG. 5 as one example of the digital equipment of this invention.

In FIG. 7, reference numeral 1 represents an image pickup unit constituted of a lens, a CCD, fundamental image pickup circuits, and the like. The image pickup unit 1 picks up a subject image and executes camera signal processing such as adjustments of luminance and color of a picked-up image. Image data processed by the image pickup unit 1 is output in the format suitable for a video processing unit 2 and a digital camera processing unit 3.

The video processing unit 2 digitizes image data supplied from the image pickup unit 1 and executes a coding process for the compression of image data in accordance with a predetermined algorithm such as a DVC format compression scheme and a MPEG scheme. The video processing unit 2 also performs the conversion of image data format suitable for transmission.

The digital camera processing unit 3 digitizes image data supplied from the image pickup unit 1, performs image processing such as adjustments of an image size and sampling, and executes a coding process for the compression of image data in accordance with a JPEG scheme or the like. The digital camera processing unit 3 also performs the conversion of image data format suitable for transmission.

Reference numeral 4 represents a switch circuit for selecting either a moving image signal sig1 from the video processing unit 2 or a still image signal sig2 from the camera processing unit 3 and supplies it via another switch circuit 22 to a 1394 serial bus I/F circuit 5. This 1394 serial bus I/F circuit 5 includes a reset circuit 19 for a 1394 serial bus 13.

Image data supplied from the video processing unit 2 or digital camera processing unit 3 can be recorded or reproduced by a recording/reproducing unit 20 without being transmitted via the 1394 bus. The reproduced data may be transmitted via the 1394 bus. The recording/reproducing unit 20 includes recording media and other necessary equipments for recording/reproducing operations.

Reference numeral 6 represents a system control circuit (controller) which is constituted of a microcomputer, a memory and the like. The controller 6 has an I/F control and address conversion circuit 7 which transfers, between the controller 6 and 1394 I/F circuit 5, node information and command/status information contained in the data transmitted from the 1394 I/F circuit to the 1394 bus 13.

Reference numeral 8 represents a first configuration ROM (CR1) which constitutes the already-described configuration ROM. This first configuration ROM stores node information for a first protocol which is used for the transmission via the 1394 bus

13 of the moving image signal sig1 and its associated command/status information, the moving image signal being obtained by a digital moving image camera/recorder (first unit) realized by a combination of the image pickup unit 1 and video processing unit 2. Proper node information in this operation state of the equipment is stored in advance in the first configuration ROM 8 during the manufacture.

Reference numeral 9 represents a second configuration ROM (CR2). This second configuration ROM stores node information for a second protocol which is used for the transmission via the 1394 bus 13 of the still image signal sig2 and its associated command/status information, the still image signal being obtained by a digital still image camera/recorder (second unit) realized by a combination of the image pickup unit 1 and camera processing unit 3. Proper node information in this operation state of the equipment is stored in advance in the second configuration ROM 9 during the manufacture.

Reference numeral 10 represents a command/status register (C & S register) used by both the first and second units and storing unit control information. Reference numeral 11 represents a control unit for controlling the operations of the first and second units in accordance with commands loaded in the C & S register 10 and also for controlling subsidiary communication protocols.

The 1394 serial bus I/F circuit 5 and controller 6 constitute the interface control device of this embodiment.

Reference numeral 12 represents a video/camera switch which selects the operation of the electronic equipment of this embodiment as viewed from the 1394 bus 13, either as the digital moving image camera/recorder (first unit) or digital still image camera/recorder (second unit).

Reference numeral 14 represents a control signal and its command/status signal for the 1394 I/F circuit 5, reference numeral 15 represents a control signal for the switch circuit 4, reference numeral 16 represents a control signal for the video processing unit 2, reference numeral 17 represents a control signal for the camera processing unit 3, reference numeral 18 represents a control signal for the image pickup unit 1, and reference numeral 21 represents a control signal for the recording/reproducing unit 20.

FIG. 8 is a diagram showing node information of CAM as viewed from the 1394 bus 13, the node information being mapped in the configuration ROM and the unit controlling command/status register. As shown, in this embodiment, the configuration ROM is constituted of the first and second configuration ROMs 8 and 9 (CR1, CR2).

Specifically, in this embodiment, in accordance with the status of the electronic equipment (whether it is used as the digital moving image camera/recorder or the digital still image camera/recorder), one of the first and second configuration ROMs 8 and 9 can be selected from the bus. Irrespective of which one of the configuration ROMs 8 and 9 is used, the C & S register 10 is used as the common area RAM.

FIG. 9 shows the contents of data to be transmitted by a subsidiary communication protocol of the digital moving image camera/recorder (first unit) or digital still image camera/recorder (second unit), the data being arranged in a data packet transmitted by the 1394 fundamental communication protocol. Each packet is added with a packet header corresponding to the fundamental communication protocol of a 1394 serial bus, and data corresponding to each subsidiary communication protocol is added to a payload area.

With reference to FIGS. 7 to 9, an operation of the digital equipment as one example of this embodiment which changes from the digital moving image camera/recorder to the digital still image camera/recorder will be described.

It is assumed that the electronic equipment of this embodiment having the structure shown in FIG. 7 operates as the digital moving image camera/recorder and communicates with another node by supplying node information onto the 1394 bus 13 via the 1394 serial bus I/F circuit 5, under the first subsidiary communication protocol stored in the first configuration ROM (CR1) 8.

In this case, the compressed moving image signal sig1 obtained by the video processing unit 2 is the data in conformity with the SD format of the DVC format, i.e., the variable length coded data after discrete cosine transformed, and is a signal having the format corresponding to the video track with sub-code data and AUX data. Such a moving image signal sig1 is transmitted via the switch circuit 4 and 1394 I/F circuit 5 in the isochronous communication mode.

At the same time, in the asynchronous communication mode, command and status information for the control of the digital moving image camera/recorder is transmitted. A reception command is stored in the C & S register 10. In accordance with the stored reception command, the control unit 11 controls the video processing unit 2 by using the control signal 16.

In this state, the digital still image camera/recorder (second unit) is transparent from the 1394 serial bus 13. In this case, for example, the 1394 serial bus I/F circuit 5 can be used as a dubbing terminal of communication to another digital moving image camera/recorder. A subsidiary communication protocol used in this case is an IEEE 1394 AV/C protocol.

In contrast with the above, if a user uses the electronic equipment of this embodiment as the digital still image camera/recorder, it may be used, for example, as a digital still image pickup equipment for an unrepresented personal computer. In this case, a protocol for the communication with this personal computer is a still image subsidiary communication protocol different from the AV/C protocol.

The outlines of an AV/C protocol and a digital still image protocol will be described. FIG. 10A shows the structure of an isochronous packet used by the AV/C protocol, and FIG. 10B shows the structure of an isochronous packet used by the digital still image protocol.

The AV/C protocol is a well known subsidiary communication protocol, and defines a real time data transfer protocol using 1394 isochronous data transfer and an isochronous data flow control. For the real time transfer, the AV/C protocol defines a CIP (Common Isochronous Packet). As shown in FIG. 10A, a CIP and real time (AV) data are stored in the data field of the isochronous packet.

The length of a source packet of the AV/C protocol is a fixed length specific to each equipment. The source packet is divided into one, two, four, or eight data blocks which are sequentially transmitted as a plurality of isochronous packets. The reception side uses a time stamp field in CIP for recovering real time data of the original packet from the divided isochronous packets.

While the equipment is under operation, an empty packet only with a packet header and a CIP header is transmitted even if there is no data to be transmitted.

The AV/C protocol prepares a FCP (Function Control Protocol) in order to control equipments on the 1394 serial buses. This FCP packet frame is transmitted by using an asynchronous packet for the control of transmission/reception of the control command.

As shown in FIG. 10B, the isochronous packet structure of the still image protocol is made to have a normal structure without a CIP and the like in the data field as in the case of the AV/C protocol. This data field stores data in the color signal format discriminated by the following modes.

Mode 0: YUV (4:4:4) format

Mode 1, Mode 3: YUV (4:2:2) format

Mode 2: YUV (4:1:1) format

Mode 4: RGB format

Mode 5: Y (Mono) format

Eight-bit pixel data is stored for each of Y, U, V, R, G and B of the above format.

The still image protocol is structured to perform only data write from the transaction layer, without having FCP as in the case of the AV/C protocol.

The description will be given for the operation after the electronic equipment of this embodiment is switched from the digital moving image camera/recorder to the digital still image camera/recorder by activating the video/camera switch 12.

Upon detection of an activation of the video/camera switch 12, the controller 6 temporarily stops the bus control of the 1394 I/F circuit 5 in order to execute the resetting of the 1394 serial bus 13 and the reconfiguration of the bus management configuration.

The digital still image camera/recorder (second unit) is reconfigured and the C & S register 10 is set for use with the digital still image camera/recorder. Next, in order to change the node information of the 1394 serial bus I/F circuit 5 from the first configuration ROM 8 to the second configuration ROM 9, the address setting of the I/F control and address conversion circuit 7 is changed. Namely, since the configuration ROMs 8 and 9 are located at different addresses in the above-described address space, the address setting is changed to select the second configuration ROM 9.

Thereafter, in order to reconfigure the management configuration of the 1394 serial bus 13 under the reset state, the bus interconnection of the 1394 serial bus I/F circuit 5 is recovered. In this manner, the electronic equipment of this embodiment is newly defined as the digital still image camera/recorder having the still image subsidiary communication protocol, in accordance with the new bus management configuration and the node information in the second configuration ROM 9. This new definition is detected by the root node which controls the bus management of the system shown in FIG. 5, and therefore recognized by the system.

In operation of the electronic equipment of this embodiment as the digital still image camera/recorder, a partner node is generally and presumably a personal computer (PC). In such a case, an image signal picked up with the image pickup unit 1 is converted by the camera processing unit 3 into image data matching the format requested by PC. This image data is supplied as a baseband image signal sig2 to PC via the switch circuit 4, 1394 serial bus I/F circuit 5, and 1394 bus 13. In this case, the above-described still image subsidiary communication protocol is used.

At the same time, PC sends a command which is stored in the C & S register 10 to set the equipment as the digital still image camera/recorder. During this time, the digital moving image camera/recorder (first unit) is transparent from the 1394 serial bus 13.

FIG. 11 is a flow chart illustrating the switching operation between the digital video (moving image) equipment and the digital camera (still image) equipment of the embodiment described above. The controller 6 has built-in software of this flow chart and the subsidiary communication protocols used for the communication by the first and second units.

Referring to FIG. 11, at Step S1 the controller 6 checks whether there is a change in the device mode, i.e., whether the video/camera switch 12 is activated. If a mode change is detected, the flow advances to Step S2 whereat the resetting operation of the 1394 serial bus 13 starts and the bus control by the 1394 serial bus I/F circuit 5 is temporarily stopped.

At Step S3 it is checked whether the digital equipment of this embodiment has been changed to the digital moving image camera/recorder (first unit) or to the digital still image camera/recorder (second unit) by the video/camera switch 12.

If changed to the digital video (moving image camera/recorder), the flow advances to Step S4 to perform the unit control corresponding to the system configuration of the digital video, at Step S5 the C & S register 10 is set for use with the digital video, and at Step S6 the address setting of the I/F control and address conversion circuit 7

is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the first configuration ROM 8.

If it is judged at Step S3 that the equipment has been changed to the digital camera (still image camera/recorder), the flow advances to Step S7 to perform the unit control corresponding to the system configuration of the digital camera, at Step S8 the C & S register 10 is set for use with the digital camera, and at Step S9 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the second configuration ROM 9.

After the processes at Steps S4 to S6 or Steps S7 to S9, the reset state of the 1394 serial bus 13 started at Step S2 is released to recover the bus connection of the 1394 serial bus I/F circuit 5. At Step S11 the root node executes a new bus management process after the system change and recognizes the equipment of this embodiment either as the moving image camera/recorder having the AV/C protocol or as the still image camera/recorder having the still image subsidiary communication protocol, in accordance with the contents of the configuration ROM 8 or 9.

As described so far in detail, according to the embodiment, different subsidiary communication protocols are selectively used to perform data communication via the 1394 serial bus I/F circuit 5. In this case, the equipment (having the structure such as shown in FIG. 5) having a plurality of units unable to operate at the same time is not required to have the C & S register independently for each unit. Even if the node information is required to be changed upon connection of a new equipment, the management configuration of the 1394 serial bus 13 can be reconfigured automatically.

As described above, the electronic equipment of this embodiment has configuration ROMs which store information on a plurality of functional units and a plurality of subsidiary communication protocols, and the system can selectively use one of a plurality of subsidiary communication protocols and one of a plurality of functional units.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

CLAIMS:

What is claimed is:

1. A device for controlling a serial bus interface interconnecting a plurality of nodes, comprising:

storage means for storing a plurality of pieces of information representative of a plurality of functions provided by one of the plurality of nodes;

selecting means for selecting one piece of the plurality of pieces of function information stored in said storage means; and

control means capable of outputting to the serial bus interface one piece of the plurality of pieces of function information selected by said selecting means,

wherein a management condition of a serial bus is reset in response to that one piece of the plurality piece of function information selected by said selecting means is changed.

2. A device according to claim 1, wherein the plurality of pieces of function information are assigned different addresses, and said selecting means selects one of the different addresses.

3. A device according to claim 1, wherein said storage means further stores a plurality of pieces of protocol information representative of a plurality of

subsidiary communication protocols corresponding to the plurality of different functions, and said control means can selectively execute the plurality of subsidiary communication protocols in addition to a fundamental communication protocol specific to the serial bus interface.

4. A device according to claim 3, wherein said selecting means further selects one piece of the plurality of pieces of protocol information, and said control means can output the protocol information selected by said selecting means to the serial bus interface.

5. A device according to claim 1, wherein the serial bus is used with the serial bus interface, and is in conformity with IEEE 1394 standards.

6. An electronic equipment connected to a serial bus interface, interconnecting a plurality of electronic equipment, comprising:

interface control means capable of executing a plurality of subsidiary communication protocols in addition to a fundamental communication protocol;

switching means for selectively executing the plurality of subsidiary communication protocols; and

selecting means for reading from another electronic equipment one piece of a plurality of pieces of protocol information representative of the plurality of subsidiary communication protocols,

wherein a management condition of a serial bus is reset in response to that one of the plurality of subsidiary communication protocols executed by said switching means is changed.

7. An electronic equipment according to claim 6, wherein the plurality of pieces or protocol information are assigned different addresses, and said selecting means selects one of the different addresses.

8. An electronic equipment according to claim 6, wherein the serial bus is used with the serial bus interface, and is in conformity with IEEE 1394 standards.

9. A device controlling a serial bus interface interconnecting a plurality of nodes, comprising:

control means capable of executing a plurality of subsidiary communication protocols in addition to a fundamental communication protocol;

switching means for selectively executing the plurality of subsidiary communication protocols; and

selecting means for selectively reading from one of the plurality of nodes one piece of a plurality of pieces of protocol information representative of the plurality of subsidiary communication protocols,

wherein a management condition of a serial bus is reset in that one of the plurality of subsidiary communication protocols executed by said switching means is changed.

10. A device according to claim 9, wherein the plurality of pieces of protocol information are assigned different addresses, and said selecting means selects one of the different addresses.

11. A device according to claim 9, wherein the serial bus is used with the serial bus interface, and is in conformity with IEEE 1394 standards.



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L2: Entry 8 of 13

File: USPT

Jan 25, 2000

DOCUMENT-IDENTIFIER: US 6018816 A

TITLE: Information processing system and method, image processing system and method, information processing apparatus and computer readable memory

Drawing Description Paragraph Right (21):

FIG. 20 is an example of a minimum format of a configuration ROM of the 1394 serial bus;

Drawing Description Paragraph Right (22):

FIG. 21 is an example of a general format of the configuration ROM of the 1394 serial bus;

Detailed Description Paragraph Right (11):

FIG. 3 shows address space of the 1394 serial bus. All the devices (nodes) connected to the 1394 serial bus have a unique 64 bit address. The 64 bit address is stored in a memory of the devices. Data communication with a designated destination device can be performed by always recognizing the node addresses of the transmitting- and receiving-side nodes.

Detailed Description Paragraph Right (14):

In the register space, the initial 512 bytes are assigned to a register core (CSR core) as a core of a Command/Status Register (CSR) architecture; the next 512 bytes, to a register of the serial bus; the next 1024 bytes, to a configuration ROM; and the remaining bytes, to a register unique to the device in a unit space.

Detailed Description Paragraph Right (15):

Generally, for the sake of simplification of bus system design for different node types, it is preferable that only the initial 2048 bytes are used for the nodes, and as a result, total 4096 bytes are used including the initial 2048 bytes for the CSR core, the register of the serial bus, the configuration ROM and the unit space.

Detailed Description Paragraph Right (20):

The respective devices (nodes) connected to the 1394 serial bus are provided with a node ID, and are recognized as nodes constructing the network. For example, when increase/decrease of the number of nodes due to connection/disconnection or power ON/OFF status of network devices, i.e., network construction changes and it is necessary to recognize a new network construction, the respective nodes detect the change of network construction, send a bus-reset signal onto the bus, and enter a mode for recognizing the new network construction. The detection of change of network construction is made by detecting change of bias voltage at the connector port 810.

WEST☐ **Generate Collection** **Print**

L2: Entry 8 of 13

File: USPT

Jan 25, 2000

US-PAT-NO: 6018816

DOCUMENT-IDENTIFIER: US 6018816 A

TITLE: Information processing system and method, image processing system and method,
information processing apparatus and computer readable memory

DATE-ISSUED: January 25, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tateyama; Jiro	Yokohama			JPX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JPX	03

APPL-NO: 9/ 053747 [PALM]

DATE FILED: April 2, 1998

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	9-087064	April 4, 1997
JP	9-115831	May 6, 1997

INT-CL: [6] G06 F 11/00, H04 L 1/08, H04 N 1/40, H04 N 1/46

US-CL-ISSUED: 714/746; 714/822, 358/462, 358/502

US-CL-CURRENT: 714/746; 358/462, 358/502, 714/822FIELD-OF-SEARCH: 714/746, 714/748, 714/749, 714/750, 714/751, 714/822, 714/5, 714/18,
714/712, 714/713, 364/265, 364/265.1, 364/265.2, 364/944.5, 364/945.5, 358/502,
358/504, 358/406, 358/462

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

☐ **Search Selected**☐ **Search ALL**

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5731882</u>	March 1998	Kawamura	358/426
<input type="checkbox"/>	<u>5802059</u>	September 1998	Hayashi	370/429
<input type="checkbox"/>	<u>5844918</u>	December 1998	Kato	714/751
<input type="checkbox"/>	<u>5845152</u>	December 1998	Anderson et al.	710/52

ART-UNIT: 275

PRIMARY-EXAMINER: Tu; Trinh L.

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper & Scinto

ABSTRACT:

A system comprising devices connected via a 1394 serial bus solves a problem that if omission of data packet occurs in isochronous transfer capable of high-speed data transfer, only data without the omitted data packet is sent to a transfer destination. A recording/reproduction device 101 repeatedly sends image data stored in a storage medium by the isochronous transfer, and a printer 102 receives the image data repeatedly sent by the isochronous transfer. If a data packet has been omitted in the received data, the omitted data packet is obtained from the data repeatedly sent by the isochronous transfer, thus the printer 102 can print an image based on the complete image data.

59 Claims, 56 Drawing figures

WEST

Generate Collection

Print

L2: Entry 8 of 13

File: USPT

Jan 25, 2000

US-PAT-NO: 6018816

DOCUMENT-IDENTIFIER: US 6018816 A

TITLE: Information processing system and method, image processing system and method, information processing apparatus and computer readable memory

DATE-ISSUED: January 25, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tateyama; Jiro	Yokohama			JPX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JPX	03

APPL-NO: 9/ 053747 [PALM]

DATE FILED: April 2, 1998

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	9-087064	April 4, 1997
JP	9-115831	May 6, 1997

INT-CL: [6] G06 F 11/00, H04 L 1/08, H04 N 1/40, H04 N 1/46

US-CL-ISSUED: 714/746; 714/822, 358/462, 358/502

US-CL-CURRENT: 714/746; 358/462, 358/502, 714/822

FIELD-OF-SEARCH: 714/746, 714/748, 714/749, 714/750, 714/751, 714/822, 714/5, 714/18, 714/712, 714/713, 364/265, 364/265.1, 364/265.2, 364/944.5, 364/945.5, 358/502, 358/504, 358/406, 358/462

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5731882</u>	March 1998	Kawamura	358/426
<input type="checkbox"/>	<u>5802059</u>	September 1998	Hayashi	370/429
<input type="checkbox"/>	<u>5844918</u>	December 1998	Kato	714/751
<input type="checkbox"/>	<u>5845152</u>	December 1998	Anderson et al.	710/52

ART-UNIT: 275

PRIMARY-EXAMINER: Tu; Trinh L.

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper & Scinto

ABSTRACT:

A system comprising devices connected via a 1394 serial bus solves a problem that if omission of data packet occurs in isochronous transfer capable of high-speed data transfer, only data without the omitted data packet is sent to a transfer destination. A recording/reproduction device 101 repeatedly sends image data stored in a storage medium by the isochronous transfer, and a printer 102 receives the image data repeatedly sent by the isochronous transfer. If a data packet has been omitted in the received data, the omitted data packet is obtained from the data repeatedly sent by the isochronous transfer, thus the printer 102 can print an image based on the complete image data.

59 Claims, 56 Drawing figures

WEST

Generate Collection

Print

L2: Entry 9 of 13

File: USPT

Nov 23, 1999

DOCUMENT-IDENTIFIER: US 5991842 A

TITLE: Communication system for providing digital data transfer, electronic equipment for transferring data using the communication system, and an interface control device

Brief Summary Paragraph Right (12):

It is another object of the present invention to provide an electronic equipment and interface control device capable of communications with various nodes via various interfaces.

Detailed Description Paragraph Right (19):

The first 512 bytes of the register space include a kernel of a known CSR architecture, and the next 512 bytes are used as a serial bus register. The specific contents of these areas are well known and the detailed description thereof is omitted. These areas and the next 1024-byte configuration ROM and a portion of a unit space are implemented on each equipment.

Detailed Description Paragraph Right (65):

It is assumed that the electronic equipment of this embodiment having the structure shown in FIG. 7 operates as the digital moving image camera/recorder and communicates with another node by supplying node information onto the 1394 bus 13 via the 1394 serial bus I/F circuit 5, under the first subsidiary communication protocol stored in the first configuration ROM (CR1) 8.

Detailed Description Paragraph Right (85):

The digital still image camera/recorder (second unit) is reconfigured and the C & S register 10 is set for use with the digital still image camera/recorder. Next, in order to change the node information of the 1394 serial bus I/F circuit 5 from the first configuration ROM 8 to the second configuration ROM 9, the address setting of the I/F control and address conversion circuit 7 is changed. Namely, since the configuration ROMs 8 and 9 are located at different addresses in the above-described address space, the address setting is changed to select the second configuration ROM 9.

Detailed Description Paragraph Right (86):

Thereafter, in order to reconfigure the management configuration of the 1394 serial bus 13 under the reset state, the bus interconnection of the 1394 serial bus I/F circuit 5 is recovered. In this manner, the electronic equipment of this embodiment is newly defined as the digital still image camera/recorder having the still image subsidiary communication protocol, in accordance with the new bus management configuration and the node information in the second configuration ROM 9. This new definition is detected by the root node which controls the bus management of the system shown in FIG. 5, and therefore recognized by the system.

Detailed Description Paragraph Right (92):

If changed to the digital video (moving image camera/recorder), the flow advances to Step S4 to perform the unit control corresponding to the system configuration of the digital video, at Step S5 the C & S register 10 is set for use with the digital video, and at Step S6 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the first configuration ROM 8.

Detailed Description Paragraph Right (93):

If it is judged at Step S3 that the equipment has been changed to the digital camera

(still image camera/recorder), the flow advances to Step S7 to perform the unit control corresponding to the system configuration of the digital camera, at Step S8 the C & S register .LO is set for use with the digital camera, and at Step S9 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the second configuration ROM 9.

Detailed Description Paragraph Right (94):

After the processes at Steps S4 to S6 or Steps S7 to S9, the reset state of the 1394 serial bus 13 started at Step S2 is released to recover the bus connection of the 1394 serial bus I/F circuit 5. At Step S11 the root node executes a new bus management process after the system change and recognizes the equipment of this embodiment either as the moving image camera/recorder having the AV/C protocol or as the still image camera/recorder having the still image subsidiary communication protocol, in accordance with the contents of the configuration ROM 8 or 9.



☐ Generate Collection Print

L2: Entry 9 of 13

File: USPT

Nov 23, 1999

DOCUMENT-IDENTIFIER: US 5991842 A

TITLE: Communication system for providing digital data transfer, electronic equipment for transferring data using the communication system, and an interface control device

Brief Summary Paragraph Right (12):

It is another object of the present invention to provide an electronic equipment and interface control device capable of communications with various nodes via various interfaces.

Detailed Description Paragraph Right (19):

The first 512 bytes of the register space include a kernel of a known CSR architecture, and the next 512 bytes are used as a serial bus register. The specific contents of these areas are well known and the detailed description thereof is omitted. These areas and the next 1024-byte configuration ROM and a portion of a unit space are implemented on each equipment.

Detailed Description Paragraph Right (65):

It is assumed that the electronic equipment of this embodiment having the structure shown in FIG. 7 operates as the digital moving image camera/recorder and communicates with another node by supplying node information onto the 1394 bus 13 via the 1394 serial bus I/F circuit 5, under the first subsidiary communication protocol stored in the first configuration ROM (CR1) 8.

Detailed Description Paragraph Right (85):

The digital still image camera/recorder (second unit) is reconfigured and the C & S register 10 is set for use with the digital still image camera/recorder. Next, in order to change the node information of the 1394 serial bus I/F circuit 5 from the first configuration ROM 8 to the second configuration ROM 9, the address setting of the I/F control and address conversion circuit 7 is changed. Namely, since the configuration ROMs 8 and 9 are located at different addresses in the above-described address space, the address setting is changed to select the second configuration ROM 9.

Detailed Description Paragraph Right (86):

Thereafter, in order to reconfigure the management configuration of the 1394 serial bus 13 under the reset state, the bus interconnection of the 1394 serial bus I/F circuit 5 is recovered. In this manner, the electronic equipment of this embodiment is newly defined as the digital still image camera/recorder having the still image subsidiary communication protocol, in accordance with the new bus management configuration and the node information in the second configuration ROM 9. This new definition is detected by the root node which controls the bus management of the system shown in FIG. 5, and therefore recognized by the system.

Detailed Description Paragraph Right (92):

If changed to the digital video (moving image camera/recorder), the flow advances to Step S4 to perform the unit control corresponding to the system configuration of the digital video, at Step S5 the C & S register 10 is set for use with the digital video, and at Step S6 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the first configuration ROM 8.

Detailed Description Paragraph Right (93):

If it is judged at Step S3 that the equipment has been changed to the digital camera

(still image camera/recorder), the flow advances to Step S7 to perform the unit control corresponding to the system configuration of the digital camera, at Step S8 the C & S register .L0 is set for use with the digital camera, and at Step S9 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the second configuration ROM 9.

Detailed Description Paragraph Right (94):

After the processes at Steps S4 to S6 or Steps S7 to S9, the reset state of the 1394 serial bus 13 started at Step S2 is released to recover the bus connection of the 1394 serial bus I/F circuit 5. At Step S11 the root node executes a new bus management process after the system change and recognizes the equipment of this embodiment either as the moving image camera/recorder having the AV/C protocol or as the still image camera/recorder having the still image subsidiary communication protocol, in accordance with the contents of the configuration ROM 8 or 9.

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Generate Collection

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L2: Entry 9 of 13

File: USPT

Nov 23, 1999

US-PAT-NO: 5991842

DOCUMENT-IDENTIFIER: US 5991842 A

TITLE: Communication system for providing digital data transfer, electronic equipment for transferring data using the communication system, and an interface control device

DATE-ISSUED: November 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takayama; Nobutoshi	Yokohama			JPX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JPX	03

APPL-NO: 8/ 917295 [PALM]

DATE FILED: August 25, 1997

INT-CL: [6] G06 F 13/00

US-CL-ISSUED: 710/105; 710/104, 710/106, 710/11

US-CL-CURRENT: 710/105; 710/104, 710/106, 710/11

FIELD-OF-SEARCH: 395/285, 395/284, 395/286, 395/831, 710/105, 710/104, 710/106, 710/11

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5506965</u>	April 1996	Naoe	395/200.39
<input type="checkbox"/>	<u>5517647</u>	May 1996	Kamada et al.	355/728
<input type="checkbox"/>	<u>5691714</u>	November 1997	Mehnert et al.	340/870.05

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Etienne; Ario

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper & Scinto

ABSTRACT:

An electronic equipment for communications with other nodes via a serial bus interface. The electronic equipment has a plurality of functions, and stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the

function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the serial bus interface. An interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

35 Claims, 12 Drawing figures

WEST

Generate Collection

Print

L2: Entry 10 of 13

File: USPT

Oct 19, 1999

DOCUMENT-IDENTIFIER: US 5968152 A

TITLE: Method and apparatus for extending key space in a plug and play ROM

Brief Summary Paragraph Right (7):

All directories in the node configuration ROMs 10 have the format shown in FIG. 2. The directory length parameter specifies the number of following quadlet entries in the directory. Each directory entry then has the format shown in FIG. 3. Each directory entry is broken down into a key field and an entry value field. The key field itself has two fields: the key type, indicating the type of directory entry, and the key value, specifying the particular directory entry, e.g., spec.sub.-- ID, unit software version, etc. The key type definitions for an embodiment according to the IEEE 1394 Serial Bus Standard are shown in Table 1, below.

Brief Summary Paragraph Right (8):

For an immediate entry, the entry value is the 24-bit value for that directory entry. Its meaning is dependent on the type of entry. For an offset entry, the entry value contains a 24-bit offset field. The offset value specifies a CSR address as a quadlet offset from the base address of the initial register space. For the leaf and directory entries, the entry value provides a 24-bit indirect offset value which specifies the address of the leaf or directory of the indirect space. The indirect offset value indirectly specifies the ROM offset address of the leaf or the directory. Thus, using the key type and key value, a specific entry in the configuration ROM 10 of a node on the serial bus can be identified.

Detailed Description Paragraph Right (1):

A method and apparatus for a plug and play serial bus interface is described. In a preferred embodiment, true plug and play operation of a computer system is provided using extended key values within control and status registers (CSRs) of configuration ROMs in the computer system. The bus architecture described herein, though described with reference to a preferred embodiment comprising components for a single computer, in general has a broader scope and could include test and measurement systems, positioning and robotic systems, and audio and video components, for example. The present invention may be applied to any arbitrarily assembled collection of nodes linked together as in a network of devices. It must also be noted that it is necessary to distinguish a node from a logical unit. Each node to reside on the bus will have associated with it at least one logical unit. In certain circumstances, a given node may be associated with multiple logical units. Usually however, there will be a one-to-one correspondence between logical units and nodes on the bus.

Detailed Description Paragraph Right (3):

Computer system 50 of FIG. 4 comprises a central processing unit (CPU) 60, a monitor 68, a printer 66, a hard drive 62, a scanner 64, a keyboard 65, and a mouse 70. The CPU 60 includes an internal hard drive 72 and a memory (not shown). Each of the devices of the computer system is coupled to a node of the serial bus. In general, the device to which a node is coupled acts as the "local host" for that node. For example, the CPU 60 is the local host for the CPU node 74; the monitor 68 is the local host for the monitor node 76; the printer 66 is the local host for the printer node 78; the hard drive 62 is the local host for the hard drive node 80; the scanner 64 is the local host for the scanner node 82; the keyboard 65 is the local host for the keyboard node 84; the mouse 70 is the local host for the mouse node 88; and the internal hard drive 72 is the local host for the internal hard drive node 90. It is not necessary for every node to have a local host, nor is it necessary that the local host always be powered.

Detailed Description Paragraph Right (8):

As discussed above, each node 74, 76, 78, 80, 82, 84, 86 and 90 of the serial bus implements a configuration ROM. Each configuration ROM is divided into a root directory, various root dependent directories, root leafs, unit directories, unit dependent directories, and unit leafs. Thus, the directories are arranged in a hierarchical fashion.

Detailed Description Paragraph Right (9):

As further described above, the CSR Architecture provides for 64 key values in directory and leaf entries within configuration ROMs. Many of these 64 values have already been assigned. For example, the IEEE 1394 Serial Bus Standard assigns key values for Module.sub.-- Vendor.sub.-- Id entries, Node.sub.-- Capabilities entries, Node.sub.-- Unique.sub.-- Id entries, Unit.sub.-- Power.sub.-- Requirements entries, and other entries. If the directory and leaf entries are limited to 64 values, support for "plug and play" ROM information and for future ROM entries will soon exhaust the available key space.

Detailed Description Paragraph Right (10):

To overcome this problem, the present invention provides for the use of extended key values within the configuration ROM hierarchical structure. For an embodiment where the configuration ROMs reside in nodes of a computer interconnect conforming to the IEEE 1394 Serial Bus Standard, two new basic key values are used to indicate (i) directories or leafs with extended key values, and (ii) the extended key value within a directory.

CLAIMS:

7. A method of providing plug and play capabilities in a system comprising:

providing a node in a plurality of devices in the system;

providing a first node in the plurality of nodes, an associated configuration memory to store configuration information; and

arranging the configuration memory in a plurality of directories, at least one of the directories having a key value, the key value indicating a unique directory entry within the configuration memory, the unique directory ent comprising an extended key value.

WEST☐

L2: Entry 10 of 13

File: USPT

Oct 19, 1999

US-PAT-NO: 5968152

DOCUMENT-IDENTIFIER: US 5968152 A

TITLE: Method and apparatus for extending key space in a plug and play ROM

DATE-ISSUED: October 19, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Staats; Erik P.	Brookdale	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 8/ 833337 [PALM]

DATE FILED: April 4, 1997

PARENT-CASE:

This application claims benefit of provisional application Ser. No. 60/015,125, filed Apr. 10, 1996.

INT-CL: [6] G06 F 17/30, G06 F 15/177

US-CL-ISSUED: 710/104; 707/200, 713/1

US-CL-CURRENT: 710/104; 707/200, 713/1

FIELD-OF-SEARCH: 395/284, 395/828, 395/800.27, 395/200.5, 395/651, 707/101, 707/200, 707/100, 707/102-104, 710/104, 710/8, 710/11, 713/1, 713/100

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4730212</u>	March 1988	Wojcik et al.	348/61
<input type="checkbox"/>	<u>4945475</u>	July 1990	Bruffey et al.	707/1
<input type="checkbox"/>	<u>5247683</u>	September 1993	Holmes et al.	395/200.51
<input type="checkbox"/>	<u>5313646</u>	May 1994	Hendricks et al.	707/101
<input type="checkbox"/>	<u>5353411</u>	October 1994	Nakaosa et al.	395/651
<input type="checkbox"/>	<u>5491817</u>	February 1996	Gopal et al.	707/200
<input type="checkbox"/>	<u>5664170</u>	September 1997	Taylor	395/200.5
<input type="checkbox"/>	<u>5734922</u>	March 1998	Hagersten et al.	395/800.37
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<input type="checkbox"/>	<u>5752243</u>	May 1998	Reiter et al.	707/3

OTHER PUBLICATIONS

Standard for A High Performance Serial Bus, IEEE Standards Document 1394, Draft 8.0v3, Oct. 16, 1995.

Information Technology--Microprocessor Systems--Control and Status Registers (CSR) Architecture for Microcomputer Buses, IEEE Standards Document 1212, 1994 edition.

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A computer system comprises a plurality of nodes interconnected by point-to-point links and forms a serial bus. At least one of the plurality of nodes includes an associated configuration memory storing configuration information. The configuration memory is arranged into a plurality of directories according to an hierarchical structure. At least one of directories has a key value which indicates a unique directory entry within the configuration memory, the unique directory entry comprising an extended key value. In one embodiment, the extended key value indicates a driver directory. In a second embodiment, the extended key indicates a protocol directory.

15 Claims, 13 Drawing figures

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L2: Entry 11 of 13

File: USPT

Mar 16, 1999

DOCUMENT-IDENTIFIER: US 5883621 A

TITLE: Device control with topology map in a digital network

Detailed Description Paragraph Right (4):

Those skilled in the art will appreciate that each of the devices 100, 106, 108, 110, 112 of the network 10 is associated with a corresponding node of the serial bus. In general, the device to which a node is coupled acts as the "local host" for that node. For example, the DSS IRD 100 is the local host for the DSS IRD node; the DVD player 106 is the local host for the DVD node; DVCR1 108 is the local host for the DVCR1 node; the MD recorder 110 is the local host for the MD recorder node; and DVCR2 112 is the local host for the DVCR2 node. It is not necessary for every node to have a local host, nor is it necessary that the local host always be powered.

Detailed Description Paragraph Right (17):

Returning to FIG. 3, step 408, after the self identification process, a device identification process is performed. During this process 408, DSS IRD 100 sends commands to all the nodes and inquires as to their respective device types. Device type information may be stored in and returned from a configuration ROM associated with each node of the serial bus as is known in the art.

Detailed Description Paragraph Right (18):

According to the responses from the nodes, DSS IRD 100 associates unique device names to the nodes automatically. For example, a DVCR will be named "DVCR". If multiple DVCRs are connected, a suffix will be attached to each of the device names as follows: DVCR1, DVCR2, etc.



Generate Collection

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L2: Entry 12 of 13

File: USPT

Sep 15, 1998

DOCUMENT-IDENTIFIER: US 5809331 A

TITLE: System for retrieving configuration information from node configuration memory identified by key field used as search criterion during retrieval

Abstract Paragraph Left (1):

A computer system comprises a plurality of nodes interconnected by point-to-point links and forms a serial bus. Upon system initialization, the bus is scanned and device-specific identification information is retrieved from command and status configuration ROMs associated with each of the plurality of nodes. In one embodiment, a search routine is used to retrieve the device specific information. The search routine begins with the definition of an iterator which is used as a place holder during the search. A simple search begins at the root directory of a hierarchical tree data structure and continues until all directories within the tree have been searched. In more complex embodiments, search relationships (i.e., direction) parameters are defined. Search criteria such as node spec.sub.-- ID and software version numbers are specified and the search is commenced. The search continues until all matching device specific information entries have been returned. The device specific information can be used to load and configure associated drivers for nodes.

Drawing Description Paragraph Right (4):

FIG. 3 illustrates the general ROM format for a configuration ROM of a serial bus according to one embodiment;

Detailed Description Paragraph Right (1):

A method and apparatus for searching and retrieving data from hierarchical tree data structures maintained within computer systems is described. In one embodiment, the method is applied to a search of control and status registers (CSRs) of configuration ROMs in a computer system. The bus architecture described herein, though described with reference to a preferred embodiment comprising components for a single computer, in general has a broader scope and could include test and measurement systems, positioning and robotic systems, and audio and video components, for example. The present invention may be applied to any arbitrarily assembled collection of nodes linked together as in a network of devices. It must also be noted that it is necessary to distinguish a node from a logical unit. Each node to reside on the bus will have associated with it at least one logical unit. In certain circumstances, a given node may be associated with multiple logical units. Usually however, there will be a one-to-one correspondence between logical units and nodes on the bus.

Detailed Description Paragraph Right (2):

Procedures of the present invention to be described operate within the environment of a computer system 5 as shown in FIG. 1. Although described with reference to a computer system 5 generally constructed in accordance with the IEEE 1394 Serial Bus Standard, the present invention is applicable to any computer system that implements the CSR configuration ROM architecture described in IEEE Standards Document 1212, 1994 edition, entitled Information Technology--Microprocessor Systems--Control and Status Registers (CSR) Architecture for Microcomputer Buses.

Detailed Description Paragraph Right (3):

Computer system 5 of FIG. 1 comprises a central processing unit (CPU) 10, a monitor 18, a printer 26, a hard drive 32, a scanner 36, a keyboard 42, and a mouse 46. The CPU 10 includes an internal hard drive 14 and a memory (not shown). Each of the devices of the computer system is coupled to a node of the serial bus. In general, the device to which a node is coupled acts as the "local host" for that node. For example,

the CPU 10 is the local host for the CPU node 12; the monitor 18 is the local host for the monitor node 16; the printer 26 is the local host for the printer node 24; the hard drive 32 is the local host for the hard drive node 30; the scanner 36 is the local host for the scanner node 34; the keyboard 42 is the local host for the keyboard node 40; the mouse 46 is the local host for the mouse node 44; and the internal hard drive 14 is the local host for the internal hard drive node 15. It is not necessary for every node to have a local host, nor is it necessary that the local host always be powered.

Detailed Description Paragraph Right (8):

FIG. 2 illustrates a typical software architecture for the computer system 5 for one embodiment. The computer system 5 software includes an operating system 100 that supports a set of application programs, including a pair of application programs 102 and 104, and a set of device driver programs for the resident and removable devices (i.e., nodes) of the computer system 5. Operating system 100 is generally stored in system memory and takes care of basic functions within computer system 5 such as handling interrupts, moving data to and from memory and peripheral devices and managing memory space. To accomplish these functions, operating system 100 provides multiple execution environments at different levels, such as task level, interrupt level, etc., as is known in the art.

Detailed Description Paragraph Right (10):

Logical device driver 106 functions as a device driver program to node 108. The logical device driver 106 processes read, write, and other commands from the application program 102 which are transferred by operating system 100. The logical device driver 106 communicates with the node 108 through a set of family services 110 functions and a set of interface module 112 functions.

Detailed Description Paragraph Right (11):

It is known in the art to provide a set of family services as interfaces between the computer operating system and logical device drivers on the one hand and physical devices of the computer system on the other hand. A device family is a collection of devices (i.e., nodes) that provide the same kind of I/O functionality. For example, the set of SCSI devices comprise the SCSI family. Likewise, nodes which conform to the IEEE 1394 Serial Bus Standard form a family of devices. In general, each family defines a family programming interface (FPI) designed to meet the particular needs of that family. An FPI provides access to a given family's services. For the example shown in FIG. 2, the family services 110 provide a set of system functions that enable application programs and device driver programs on the computer system 5 to access the removable devices coupled to the bus.

Detailed Description Paragraph Right (13):

For an embodiment conforming to the IEEE 1394 Serial Bus Standard, each transaction capable node 12, 15, 16, 24, 32, 34, 40 and 44 of the serial bus implements a configuration ROM. The configuration ROM is a nonvolatile memory which stores critical boot information which is accessed during bus initialization as described below. The boot information is stored in the Name Registry and used to identify the appropriate driver software to be loaded for the node of interest.

Detailed Description Paragraph Right (14):

FIG. 3 illustrates the general ROM format for each configuration ROM 50 of the serial bus. For one embodiment, the node configuration ROMs 50 reside within the address space of the serial bus in accordance with the IEEE 1394 Serial bus Standard. As shown, the configuration ROM 50 is divided into a root directory 52, various root dependent directories 54, root leafs 56, unit directories 58, unit dependent directories 60, and unit leafs 62. Thus, the directories are arranged in a hierarchical fashion. Within this structure, directories may have "children", "parents" and "siblings".

Detailed Description Paragraph Right (16):

All directories in the node configuration ROMs 50 have the format shown in FIG. 4. The directory length parameter specifies the number of following quadlet entries in the directory. Each directory entry then has the format shown in FIG. 5. Each directory entry is broken down into a key field and an entry value field. The key field itself has two fields: the key type, indicating the type of directory entry, and the key

value, specifying the particular directory entry, e.g., spec.sub.-- ID, unit software version, etc. The key type definitions for a preferred embodiment according to the IEEE 1394 Serial Bus Standard are shown in Table 1, below.

Detailed Description Paragraph Right (17):

For an immediate entry, the entry value is the 24-bit value for that directory entry. Its meaning is dependent on the type of entry. For an offset entry, the entry value contains a 24-bit offset field. The offset value specifies a CSR address as a quadlet offset from the base address of the initial register space. For the leaf and directory entries, the entry value provides a 24-bit indirect offset value which specifies the address of the leaf or directory of the indirect space. The indirect offset value indirectly specifies the ROM offset address of the leaf or the directory. Thus, using the key type and key value, a specific entry in the configuration ROM 50 of a node on the serial bus can be identified.

Detailed Description Paragraph Right (18):

The present invention provides a method for searching the configuration ROMs 50 of the nodes on a serial bus. In one embodiment, a method of searching for and retrieving node software version and spec.sub.-- ID information is provided. This information can then be used by computer system 5 to load appropriate driver software for the nodes of the bus.

Detailed Description Paragraph Right (19):

The search routine, in one embodiment, is provided with a pointer to the CSR configuration ROM of a specified node within the address space of the serial bus. Search parameters are defined. The search parameters correspond to the key types and key values defined for the node software version number and spec.sub.-- ID. Using these parameters, the search routine scans the address space of the configuration ROM and returns with matches for the given search parameters.

WEST☐ **Generate Collection** **Print**

L2: Entry 12 of 13

File: USPT

Sep 15, 1998

US-PAT-NO: 5809331

DOCUMENT-IDENTIFIER: US 5809331 A

TITLE: System for retrieving configuration information from node configuration memory identified by key field used as search criterion during retrieval

DATE-ISSUED: September 15, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Staats; Erik P.	Brookdale	CA		
Lash; Robin D.	Milpitas	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 8/ 626462 [PALM]

DATE FILED: April 1, 1996

INT-CL: [6] G06 F 13/00, G06 F 13/24, G06 F 13/36

US-CL-ISSUED: 395/830; 395/500, 395/872, 395/284, 395/681

US-CL-CURRENT: 710/10; 703/22, 709/321, 710/104, 710/52

FIELD-OF-SEARCH: 395/651, 395/681, 395/872, 395/830, 395/500, 395/284

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

☐ **Search Selected**☐ **Search ALL**

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4020466</u>	April 1977	Cordi et al.	340/172.5
<input type="checkbox"/>	<u>5202986</u>	April 1993	Nickel	395/600
<input type="checkbox"/>	<u>5343471</u>	August 1994	Cassagnol	370/85.13
<input type="checkbox"/>	<u>5586268</u>	December 1996	Chen et al.	395/250
<input type="checkbox"/>	<u>5598563</u>	January 1997	Spies	395/652
<input type="checkbox"/>	<u>5630076</u>	May 1997	Saulpaugh et al.	395/284
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ART-UNIT: 272

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Perveen; Rehana

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A computer system comprises a plurality of nodes interconnected by point-to-point links and forms a serial bus. Upon system initialization, the bus is scanned and device-specific identification information is retrieved from command and status configuration ROMs associated with each of the plurality of nodes. In one embodiment, a search routine is used to retrieve the device specific information. The search routine begins with the definition of an iterator which is used as a place holder during the search. A simple search begins at the root directory of a hierarchical tree data structure and continues until all directories within the tree have been searched. In more complex embodiments, search relationships (i.e., direction) parameters are defined. Search criteria such as node spec.sub.-- ID and software version numbers are specified and the search is commenced. The search continues until all matching device specific information entries have been returned. The device specific information can be used to load and configure associated drivers for nodes.

12 Claims, 6 Drawing figures



US006038625A

United States Patent [19]**Ogino et al.**[11] **Patent Number:** **6,038,625**[45] **Date of Patent:** **Mar. 14, 2000**

[54] **METHOD AND SYSTEM FOR PROVIDING A DEVICE IDENTIFICATION MECHANISM WITHIN A CONSUMER AUDIO/VIDEO NETWORK**

[75] **Inventors:** Hiroshi Ogino, Sunnyvale; Feng (Frank) Zou, Milpitas, both of Calif.

[73] **Assignees:** Sony Corporation of Japan, Tokyo, Japan; Sony Electronics, Inc., Park Ridge, N.J.

[21] **Appl. No.:** 09/003,111

[22] **Filed:** Jan. 6, 1998

[51] **Int. Cl.⁷** G06F 13/00

[52] **U.S. Cl.** 710/104; 710/8; 710/9; 710/10; 709/302; 712/1; 712/208

[58] **Field of Search** 710/43, 104, 8, 710/9, 10, 2; 712/208, 1; 709/302, 300, 220, 221, 222; 348/552

[56] **References Cited**

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404038549A 2/1992 Japan G06F 13/00

Primary Examiner—Xuan M. Thai

Attorney, Agent, or Firm—Wagner, Murabito & Hao LLP

[57] **ABSTRACT**

A method and system for providing a device identification mechanism within a consumer electronics based audio/video network. Several consumer electronics products, e.g., television, VCR, tuner, set-top box (e.g., intelligent receiver/decoder, IRD), DVTRs, PCs, DVD players (digital video disk), etc., can be coupled within the network to communicate together via a standard bus (e.g., IEEE 1394 serial communication bus). In one embodiment, the HAVI network offers unique advantages consumer electronic vendors because the architecture offers for the home network many of the advantages of existing computer system networks. Specifically, interconnected devices can share resources and provide open, well defined APIs that allow ease of development for third party developers. The present invention provides a mechanism whereby a global unique identifier (GUID) is associated with each device of the HAVI network. A low level driver constructs a GUID list of each device on the HAVI network. The order of the GUID entries in the GUID list (e.g., the index) matches the physical identifiers assigned to the devices by the 1394 serial bus. Although the physical identifiers can change on bus reset, the GUID values are constant and are used for device communication. Speed map and topology map information is maintained based on the physical identifier information and therefore translations between GUIDs and physical identifiers are efficiently performed by the present invention when referencing speed map and topology information for an application.

22 Claims, 26 Drawing Sheets

220

APPLICATION LAYER



US006185622B1

(12) **United States Patent**
Sato

(10) Patent No.: **US 6,185,622 B1**
(45) Date of Patent: **Feb. 6, 2001**

(54) **ELECTRONIC APPARATUS,
COMMUNICATION SPEED INFORMATION
COLLECTION METHOD,
COMMUNICATION METHOD BETWEEN
ELECTRONIC APPARATUS AND
RECORDING MEDIUM**

(75) Inventor: **Makoto Sato, Tokyo (JP)**

(73) Assignee: **Sony Corporation, Tokyo (JP)**

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/057,392**

(22) Filed: **Apr. 8, 1998**

(30) **Foreign Application Priority Data**

Apr. 15, 1997 (JP) 9-096873

(51) Int. Cl.⁷ **G06F 13/00**

(52) U.S. Cl. **709/233**

(58) Field of Search **709/200, 232,
709/233, 328**

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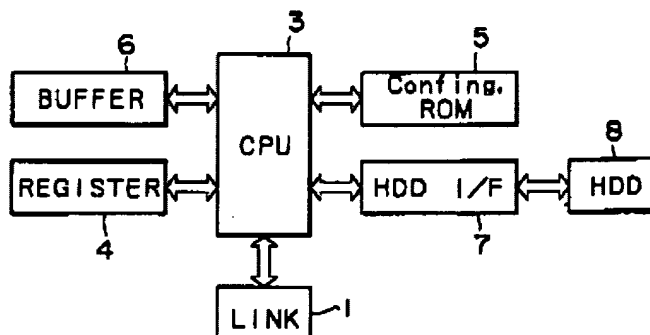
Primary Examiner—Robert B. Harrell

(74) Attorney, Agent, or Firm—Frommer Lawrence & Haug, LLP; William S. Frommer

(57) **ABSTRACT**

The invention provides an electronic apparatus, a communication speed information collection method, a communication method between electronic apparatus and a recording medium which can minimize the possibility of drop of a communication speed by a performance of a repeating node and by which communication speed information having a high degree of reliability can be obtained. When bus resetting occurs, a parental relationship of nodes is determined automatically, and the nodes send out self ID packets in a predetermined order to a 1,394 serial bus. One of the nodes which has been determined as a bus manager produces a speed map using maximum communication speed information of physical layer controllers written in the self ID packets sent out from the nodes. Then, the node reads out configuration ROMs of the other nodes and modifies the information regarding any node wherein the maximum communication speed of the link layer controller is lower than the maximum communication speed of the physical layer controller.

16 Claims, 5 Drawing Sheets





US005809331A

United States Patent [19][11] **Patent Number:** **5,809,331****Staats et al.**[45] **Date of Patent:** **Sep. 15, 1998**

[54] **SYSTEM FOR RETRIEVING CONFIGURATION INFORMATION FROM NODE CONFIGURATION MEMORY IDENTIFIED BY KEY FIELD USED AS SEARCH CRITERION DURING RETRIEVAL**

[75] **Inventors:** Erik P. Staats, Brookdale; Robin D. Laah, Milpitas, both of Calif.

[73] **Assignee:** Apple Computer, Inc., Cupertino, Calif.

[21] **Appl. No.:** 626,462

[22] **Filed:** Apr. 1, 1996

[51] **Int. Cl.** G06F 13/00; G06F 13/24; G06F 13/35

[52] **U.S. Cl.** 395/830; 395/500; 395/872; 395/284; 395/681

[58] **Field of Search** 395/651, 651, 395/872, 830, 500, 284

[56] **References Cited****U.S. PATENT DOCUMENTS**

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High Performance Serial Bus Working Group of the Microprocessor and Microcomputer Standards Committee, "P1394 Standard for a High Performance Serial Bus", P1394 Draft 8.0v3, pp. 1-364, (Oct. 16, 1995).

Apple Computer, "Inside Macintosh, Devices", Nov. 1994, pp. 3.1-3.48.

"Information Technology—Microprocessor Systems—Control and Status Registers (CSR) Architecture for Microcomputer Buses" IEEE 1212, 1994.

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Apple Computer, "Designing PCI Cards and Drivers for Power Macintosh Computers", Mar. 1995, pp. 1-366.

Apple Computer, Inc., "Interim Draft, Designing PCI Cards and Drivers for Power Macintosh Computers", A8 Draft—Preliminary Information, pp. 1-372, (Mar. 9, 1995).

Primary Examiner—Thomas C. Lee

Assistant Examiner—Rehana Perveen

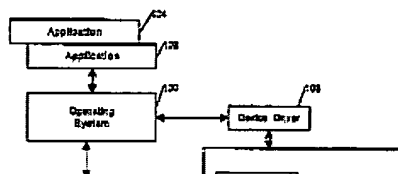
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57]

ABSTRACT

A computer system comprises a plurality of nodes interconnected by point-to-point links and forms a serial bus. Upon system initialization, the bus is scanned and device-specific identification information is retrieved from command and status configuration ROMs associated with each of the plurality of nodes. In one embodiment, a search routine is used to retrieve the device specific information. The search routine begins with the definition of an iterator which is used as a place holder during the search. A simple search begins at the root directory of a hierarchical tree data structure and continues until all directories within the tree have been searched. In more complex embodiments, search relationships (i.e., direction) parameters are defined. Search criteria such as node spec_ID and software version numbers are specified and the search is commenced. The search continues until all matching device specific information entries have been returned. The device specific information can be used to load and configure associated drivers for nodes.

12 Claims, 4 Drawing Sheets





US006353868B1

(12) United States Patent
Takayama et al.**(10) Patent No.: US 6,353,868 B1**
(45) Date of Patent: Mar. 5, 2002**(54) DIGITAL CAMERA CONTROLLING**
COMMUNICATION BY MULTIPLE
FUNCTION UNITS**(75) Inventors:** Nobutoshi Takayama, Yokohama;
Masamichi Ito, Tokyo, both of (JP)**(73) Assignee:** Canon Kabushiki Kaisha, Tokyo (JP)**(*) Notice:** Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.**(21) Appl. No.:** 09/614,547**(22) Filed:** Jul. 12, 2000**Related U.S. Application Data****(62)** Division of application No. 09/414,319, filed on Oct. 7,
1999, now Pat. No. 6,138,196, which is a division of
application No. 08/917,295, filed on Aug. 25, 1997, now Pat.
No. 5,991,842.**(30) Foreign Application Priority Data**

Aug. 27, 1996 (JP) 8-225183

(51) Int. Cl.⁷ G06F 13/00; G06F 13/42**(52) U.S. Cl.** 710/129; 710/105; 710/106;
710/62; 710/11; 358/1.15**(58) Field of Search** 710/105, 104,
710/106, 11, 62, 101, 129; 348/220; 709/238;
370/463, 912; 358/1.15**(56) References Cited****U.S. PATENT DOCUMENTS**

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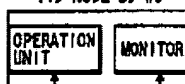
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Primary Examiner—Gopal C. Ray**(74) Attorney, Agent, or Firm**—Fitzpatrick, Cella, Harper &
Scinto**(57) ABSTRACT**

An electronic equipment for communications with other nodes via a serial bus interface. The electronic equipment has a plurality of functions, and stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the serial bus interface. An interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

64 Claims, 10 Drawing Sheets

TV/NODE B/#3



CAM/NODE A/#20

PC/NODE C/#9



US006185622B1

(12) **United States Patent**
Sato

(10) Patent No.: **US 6,185,622 B1**
(45) Date of Patent: **Feb. 6, 2001**

(54) **ELECTRONIC APPARATUS,
COMMUNICATION SPEED INFORMATION
COLLECTION METHOD,
COMMUNICATION METHOD BETWEEN
ELECTRONIC APPARATUS AND
RECORDING MEDIUM**

(75) Inventor: **Makoto Sato, Tokyo (JP)**

(73) Assignee: **Sony Corporation, Tokyo (JP)**

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/057,392**

(22) Filed: **Apr. 8, 1998**

(30) **Foreign Application Priority Data**

Apr. 15, 1997 (JP) 9-096873

(51) Int. Cl.⁷ **G06F 13/00**

(52) U.S. Cl. **709/233**

(58) Field of Search **709/200, 232,
709/233, 328**

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,038,625 * 3/2000 Ogino et al. 710/104

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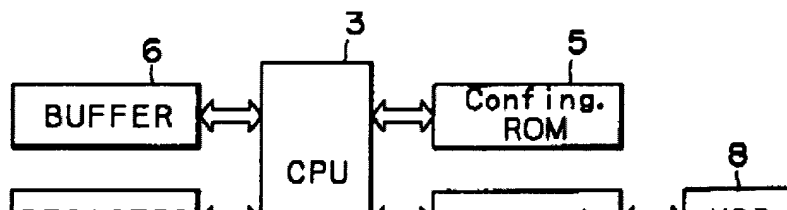
Primary Examiner—Robert B. Harrell

(74) *Attorney, Agent, or Firm—Frommer Lawrence & Hang, LLP; William S. Frommer*

(57) **ABSTRACT**

The invention provides an electronic apparatus, a communication speed information collection method, a communication method between electronic apparatus and a recording medium which can minimize the possibility of drop of a communication speed by a performance of a repeating node and by which communication speed information having a high degree of reliability can be obtained. When bus resetting occurs, a parental relationship of nodes is determined automatically, and the nodes send out self ID packets in a predetermined order to a 1,394 serial bus. One of the nodes which has been determined as a bus manager produces a speed map using maximum communication speed information of physical layer controllers written in the self ID packets sent out from the nodes. Then, the node reads out configuration ROMs of the other nodes and modifies the information regarding any node wherein the maximum communication speed of the link layer controller is lower than the maximum communication speed of the physical layer controller.

16 Claims, 5 Drawing Sheets





US006160796A

United States Patent [19]

Zou

[11] **Patent Number:** 6,160,796[45] **Date of Patent:** Dec. 12, 2000

[54] **METHOD AND SYSTEM FOR UPDATING
DEVICE IDENTIFICATION AND STATUS
INFORMATION AFTER A LOCAL BUS
RESET WITHIN A HOME AUDIO/VIDEO
NETWORK**

[75] **Inventor:** Feng (Frank) Zou, Milpitas, Calif.

[73] **Assignees:** Sony Corporation of Japan, Tokyo,
Japan; Sony Electronics, Inc., Park
Ridge, N.J.

[21] **Appl. No.:** 09/003,118

[22] **Filed:** Jan. 6, 1998

[51] **Int. Cl.⁷** G06F 13/00

[52] **U.S. CL.** 370/257; 710/104

[58] **Field of Search** 370/254, 257,
370/389, 390, 402, 408, 437, 438, 439,
451, 453, 457; 709/221, 222, 300; 710/8,
9, 10, 11, 104

[56] **References Cited****U.S. PATENT DOCUMENTS**

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5,420,573	5/1995	Tanaka et al.	340/825.24
5,537,605	7/1996	Teece	395/800
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Primary Examiner—Chi H. Pham

Assistant Examiner—Frank Duong

Attorney, Agent, or Firm—Wagner Murabito & Hao LLP

[57] **ABSTRACT**

A method and system for updating device identification and status information in response to a local bus reset within a home audio/video network. Several consumer electronics products, e.g., television, VCR, tuner, set-top box (e.g., intelligent receiver/decoder, IRD), DVRs, PCs, DVD players (digital video disk), etc., can be coupled within the network to communicate together via a standard bus (e.g., IEEE 1394 serial communication bus). In one embodiment, the communication architecture used is the home audio/visual initiative (HAVI) format. The HAVI network offers unique advantages consumer electronic vendors because the architecture offers for the home network many of the advantages of existing computer system networks. Namely, interconnected devices can share resources and provide open, well defined APIs that allow ease of development for third party developers. The present invention provides a mechanism whereby devices of the network are informed of the current status of the network after a local bus reset caused when a device is inserted into the network or when a device is removed from the network. After a reset, a new GUID list is generated by a driver and passed to a high level program. The high level program then compares the new GUID list with its own copy of an older version and generates a list of devices added to the network after the bus reset and a list of devices removed from the network after the bus reset. This information is then forwarded to all devices on the network that previously specified certain call back information regarding current device status.

20 Claims, 26 Drawing Sheets

200

APPLICATION LAYER



US006141767A

United States Patent [19]

Hu et al.

[11] **Patent Number:** 6,141,767[45] **Date of Patent:** Oct. 31, 2000

[54] **METHOD OF AND APPARATUS FOR VERIFYING RELIABILITY OF CONTENTS WITHIN THE CONFIGURATION ROM OF IEEE 1394-1995 DEVICES**

[75] **Inventors:** Qi Hu, Santa Clara; Hisato Shima, Saratoga, both of Calif.

[73] **Assignees:** Sony Corporation, Tokyo, Japan; Sony Electronics, Inc., Park Ridge, N.J.

[21] **Appl. No.:** 09/055,132

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[52] **U.S. Cl.** 714/1; 365/201

[58] **Field of Search** 714/1, 2, 5, 7, 714/20, 25, 27, 31, 39, 54, 4, 30, 718, 736; 365/185.22, 201; 364/491

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[57] **ABSTRACT**

A graphical user interface is used to display contents of a configuration memory and includes a hierarchical window illustrating directories and entries within the configuration memory including the relationships between the directories and entries and a data window for displaying data stored within the configuration memory and signalling errors corresponding to the data. The errors are determined by processing the data being displayed to determine a reference value for each entry within the data and to determine if any offset value, pointer value and count value included within any entry references a memory location outside of a boundary of the memory. The reference value specifies a number of times each entry is referenced. Errors are signalled within the data window by displaying entries corresponding to errors in a first color and entries which do not include errors in a second color. The system further includes a bus structure node circuit for coupling the system to other devices over a bus structure. Appropriate headings of directories and entries are displayed with the data in the data window. The bus structure is preferably an IEEE 1394-1995 serial bus.

30 Claims, 12 Drawing Sheets

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<input type="checkbox"/> ROM1	<input type="checkbox"/> <input type="checkbox"/>
<input checked="" type="checkbox"/> Rom Data	

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United States Patent [19][11] **Patent Number:** 6,138,196

Takayama et al.

[45] **Date of Patent:** Oct. 24, 2000

[54] **COMMUNICATION SYSTEM FOR PROVIDING DIGITAL DATA TRANSFER, ELECTRONIC EQUIPMENT FOR TRANSFERRING DATA USING THE COMMUNICATION SYSTEM, AND AN INTERFACE CONTROL DEVICE**

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Related U.S. Application Data

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[52] **U.S. Cl.** 710/105; 710/104; 710/106;
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[58] **Field of Search** 710/105, 104,
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370/463, 912; 379/88.13

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[57] ABSTRACT

An electronic equipment for communications with other nodes via a serial bus interface. The electronic equipment has a plurality of functions, and stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the serial bus interface. An interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

11 Claims, 10 Drawing Sheets